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Understanding the switching mechanism of interfacial phase change memory

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ABSTRACT

Phase Change Memory (PCM) is a leading candidate for next generation data storage, but it typically suffers from high switching (RESET) current density (20–30 MA/cm^2). Interfacial Phase Change Memory (IPCM) is a type of PCM using multilayers of Sb_2Te_3/GeTe, with up to 100× lower reported RESET current compared to the standard $Ge_2Sb_2Te_5$-based PCM. Several hypotheses involving fundamentally new switching mechanisms have been proposed to explain the low switching current densities, but consensus is lacking. Here, we investigate IPCM switching by analyzing its thermal, electrical, and fabrication dependencies. First, we measure the effective thermal conductivity (~0.4 W m^{-1} K^{-1}) and thermal boundary resistance (~3.4 m^2 K GW^{-1}) of Sb_2Te_3/GeTe multilayers. Simulations show that IPCM thermal properties account only for an ~13% reduction of current vs standard PCM and cannot explain previously reported results. Interestingly, electrical measurements reveal that our IPCM RESET indeed occurs by a melt-quench process, similar to PCM. Finally, we find that high deposition temperature causes defects including surface roughness and voids within the multilayer films. Thus, the substantial RESET current reduction of IPCM appears to be caused by voids within the multilayers, which migrate to the bottom electrode interface by thermophoresis, reducing the effective contact area. These results shed light on the IPCM switching mechanism, suggesting that an improved control of layer deposition is necessary to obtain reliable switching.

I. INTRODUCTION

Phase change memory (PCM) is a class of emerging nonvolatile memory that combines several attractive properties, including random access, multilevel analog states,[1] excellent scalability (down to approximately a few square nanometers),[2–6] fast reading and writing,[7,8] reasonable endurance (as high as ~2×10^{12} cycles[9]), and unipolar switching, while being compatible with back-end-of-the-line (BEOL) silicon processing. Its unique balance of cost-per-bit vs reading and writing time within the memory hierarchy makes PCM a leading candidate for storage class memory applications where cost and speed trade-offs between dynamic random-access memory (DRAM) and NAND flash are desired.[10] Other compelling applications include neuromorphic analog computing systems, which have been demonstrated[11,12] by leveraging device properties not available in conventional incumbent memories, such as static random-access memory (SRAM), DRAM, NAND flash, or hard disk drives.

The primary disadvantage of PCMs with respect to other nonvolatile memories is their high RESET current density, J_{RESET} (and consequentially, RESET power and energy), which involves the switching phase change material layer (e.g., GST) to be heated above its melting temperature, T_m. For example, the energy required to RESET PCMs is greater than the typical energy required to charge interconnects for a random one-bit switch in a 1024 by 1024

memory array.[13] On the other hand, other types of emerging nonvolatile memory, including resistive random-access memory (RRAM), conductive bridge random-access memory (CBRAM), and spin transfer-torque random-access memory (STT-MRAM), have at least a few demonstrations of switching energies below the interconnect charging energy.[14–16] This indicates that PCMs still have an opportunity to effectively reduce system-level energy consumption by means of clever device-level engineering. For example, reducing the cell volume and reducing the programming pulse widths[17] are two very effective ways to decrease the RESET energy by over an order of magnitude. However, these methods do not reduce J_{RESET}, which is still around 20–30 MA/cm^2 in typical PCMs. Such current densities cannot be matched by most memory selectors (Sec. 1 in the supplementary material), which are devices required to prevent unwanted leakage paths in memory arrays.[18,19] Thus, selector devices for PCM would require separate patterning with a larger footprint, resulting in higher costs.

Recently, a new class of PCM called interfacial phase change memory (IPCM) has been reported with significant reduction of J_{RESET}, from 35% to 99% compared to standard PCM cells (Sec. 2 in the supplementary material).[20–25] IPCM has two distinguishing characteristics compared to conventional PCM: First, the structure consists of thinly stacked multilayers (generally a few nanometers each) of chalcogenides (Sb_2Te_3 and GeTe being the most common) instead of a uniform chalcogenide layer (typically $Ge_2Sb_2Te_5$, abbreviated as GST). Second, IPCMs are typically deposited at higher temperatures, ranging from 200 to 250 °C.[21,22,26] Several hypotheses involving a fundamentally new switching mechanism have been proposed. Most involve a crystalline to crystalline transition, rather than a crystalline to amorphous transition seen in standard PCMs. The higher deposition temperature is suggested to play a role in growing epitaxial or semiepitaxial films with crystal structures that enable this unique switching mechanism proposed for IPCM.[27] The driving force and atomic coordination (including the actual phase of the different states) that lead to the switching between different resistive states of IPCM remain under debate. Arguments of the driving force include charge injection,[28,29] electric field,[30] thermal activation,[31] and a combination of Joule heating and electric field.[32] The atomic configurations of the low resistance state (LRS) are also debated between Ferro (Ge–Te–Ge–Te)[31,33] and Petrov (Ge–Te–Te–Ge) structures.[22,26,29] The primary objective of this work is to elucidate the physical origin of low J_{RESET} as well as its large variations seen in IPCMs by analyzing thermal, electrical, and process conditions.

II. THERMAL ANALYSIS

Conventional PCMs RESET by a melt-quench process in which the switching phase change material layer (e.g., GST) is heated above T_m, followed by a rapid quench that puts the GST in an amorphous state. Strategic spatial allocation of thermal resistances has previously been shown to play a key role in confining heat and reducing J_{RESET}.[34–36] Since IPCMs have a high cross-plane interfacial density, one possible cause of low J_{RESET} could be owed to enhanced thermal confinement due to lower effective thermal conductivity ($=\kappa_{eff}$) of the multilayer stack. [We define κ_{eff} as the cross-plane thermal conductivity of the IPCM layers including "internal" Sb_2Te_3/GeTe thermal boundary resistances (TBR) but excluding "external" TBR to the top electrode (TE) and bottom electrode (BE), etc.] To assess this hypothesis, we first measure κ_{eff} as a function of IPCM period thickness ($=d$), which allows us to estimate the contribution of the interfaces to the total thermal resistance. Then, we use finite element simulations to analyze how modifying κ_{eff} impacts the current and power density to heat a fixed volume within the memory cell. Since Joule self-heating is always present regardless of the actual switching mechanism, this allows us to evaluate whether melt-quench RESET applies to IPCMs, without making specific assumptions involving the proposed mechanisms.

Figure 1(a) shows a cross-sectional schematic of the IPCM samples used for thermal characterization, along with their process conditions (Sec. 3 in the supplementary material). Time domain thermoreflectance (TDTR) was used to measure κ_{eff} at room temperature (RT).[37–39] Figure 1(b) reveals that κ_{eff} monotonically decreases with decreasing period thickness, suggesting that the interfacial thermal resistance is indeed significant compared to the volumetric resistances of the individual layers. To extract the TBR between Sb_2Te_3 and GeTe, we plot the thermal resistance of a single period vs period thickness as shown in Fig. 1(c) and use a series resistor model (Sec. 4 in the supplementary material); the TBR is estimated to be ~3.4 m^2 K GW^{-1}. This is noticeably lower than prior TBR studies of GST/TiN (~26 m^2 K GW^{-1})[40] and GST/SiO_2 interfaces (~28 m^2 K GW^{-1}),[41] potentially due to intermixing at the Sb_2Te_3/GeTe interface. Figure 1(d) plots the fractional contribution of the TBR to the unit period film thermal resistance, as a function of period thickness. We find that interfaces constitute nearly 50% of the thermal resistance in the thinnest period sample, $[4\text{ nm } Sb_2Te_3\text{:}1\text{ nm GeTe}]_{12}$. This sample has a thermal conductivity $\kappa_{eff} \sim 0.4$ W m^{-1} K^{-1}; in comparison, literature values for $Ge_2Sb_2Te_5$ films processed (200 °C) and measured (20 °C) at similar temperatures are close to ~0.5 W m^{-1} K^{-1}, higher than that of IPCM.[42] The lower κ_{eff} of the IPCM compared to GST-based PCM originates at least in part from the thermal resistance of the interfaces, as shown in Fig. 1(d).

The impact of κ_{eff} on J_{RESET} of IPCM was subsequently assessed by finite element simulations, in Fig. 2(a). Voltage pulses with incremental amplitudes were applied across the top and the bottom electrode until a constant fraction of the chalcogenide layer volume was heated above T_m. Further details on simulation assumptions and methodologies are delineated in Sec. 5 in the supplementary material. Figure 2(b) shows the simulated J_{RESET} (blue circles) and RESET power density, P_{RESET} (orange crosses), as a function of κ_{eff} over κ_{GST}. From these simulations, we deduce decreasing κ_{eff} from GST to the best case (lowest κ_{eff}) IPCM results in only ~13% reduction of J_{RESET} and ~17% reduction of P_{RESET}. From a purely thermal standpoint, our simulations estimate that to reduce J_{RESET} by ~10×, κ_{eff} must be reduced by ~100×, which is unphysical because it is much less than the thermal conductivity of dry air (~0.023 W m^{-1} K^{-1}).[43]

Considering the magnitude of previously reported J_{RESET} reductions shown in Sec. 2 in the supplementary material (100× reduction as an example), we conclude that the modest difference in thermal properties alone cannot explain the observed J_{RESET} reductions. We note that due to the lack of Sb_2Te_3, GeTe, and Sb_2Te_3/TiN interface temperature-dependent electrical resistivity studies above room

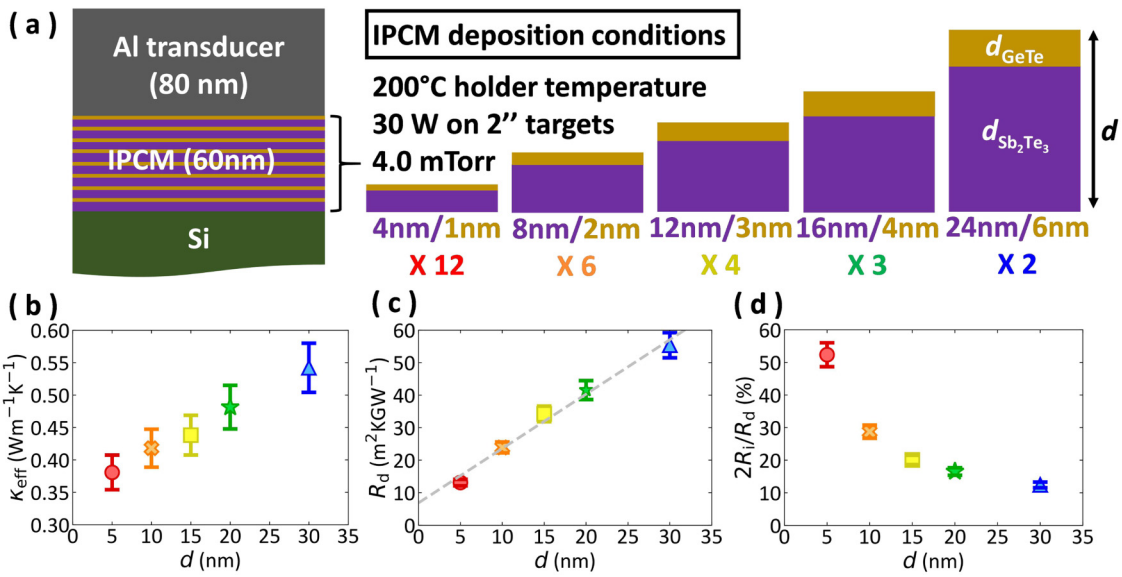

FIG. 1. (a) Samples and process conditions used for IPCM film thermal characterization. The individual layers are alternating Sb_2Te_3 and GeTe, as labeled. The relative film thicknesses are fixed to $d_{Sb_2Te_3} = 4d/5$ and $d_{GeTe} = d/5$, where d is the period thickness. (b) Dependence of IPCM cross-plane thermal conductivity, κ_{eff}, on period thickness, d. (c) Measured R_d vs d and linear fit for TBR (=R_i) extraction of the Sb_2Te_3/GeTe interface. R_d is the thermal resistance of a single period of a [Sb_2Te_3:GeTe] IPCM stack. The vertical intercept corresponds to $2R_i$. (d) TBR contribution to the IPCM stack thermal resistance (in %), as a function of period thickness.

temperature,[44] our simulations assumed electrical resistivity of GST[45] and GST/metal interfaces.[46] If T_m of Sb_2Te_3 or GeTe were lower than GST and had higher electrical resistivities, it might be possible to reduce J_{RESET} even further, but since bulk T_m values are comparable or higher (GeTe: ~720 °C, Sb_2Te_3: ~620 °C, and GST: ~620 °C), we do not expect 100-fold J_{RESET} reduction even with these modifications.

III. ELECTRICAL ANALYSIS

Next, to assess IPCM electrical characteristics, we fabricate and test mushroom-type memory cells with 80 nm diameter TiN bottom electrode (BE) and [4 nm Sb_2Te_3:1 nm GeTe]$_{10}$ stack (with Sb_2Te_3 as the starting layer contacting the BE), as detailed in Sec. 3 in the supplementary material. Reference PCM cells with 50 nm of $Ge_2Sb_2Te_5$ and identical BE conditions were also fabricated for comparison. The chalcogenide layers for both PCM and IPCM devices were sputtered at 200 °C in Ar ambient with a pressure of 4 mTorr. Figure 3(a) shows DC read resistance vs current measurements (electrical measurement setup and methodologies are described in Sec. 6 in the supplementary material). Well-behaved PCMs have $J_{RESET} \sim 25$ MA/cm^2, while IPCMs RESET at ~30 MA/cm^2 current density. IPCMs had a noticeably higher cycle-to-cycle variation (Sec. 7 in the supplementary material). Interestingly, we were also able to measure low J_{RESET} IPCMs from a different device on the same chip. The low J_{RESET} device degraded soon after and we were

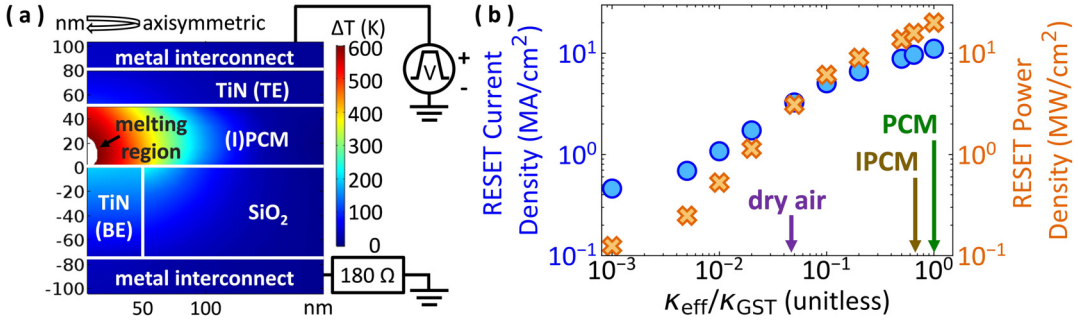

FIG. 2. (a) Model used for finite element simulations to assess the impact of κ_{eff} toward RESET current and power density. The device is cylindrically symmetric around the left vertical axis. (b) Simulated effect of reducing κ_{eff} (as the ratio $\kappa_{eff}/\kappa_{GST}$) on the reduction of current density (blue circles) and power density (orange crosses) required to heat a small (fixed) fraction of the switching layer above T_m (soft RESET). Large J_{RESET} reduction requires unrealistic κ_{eff} reduction.

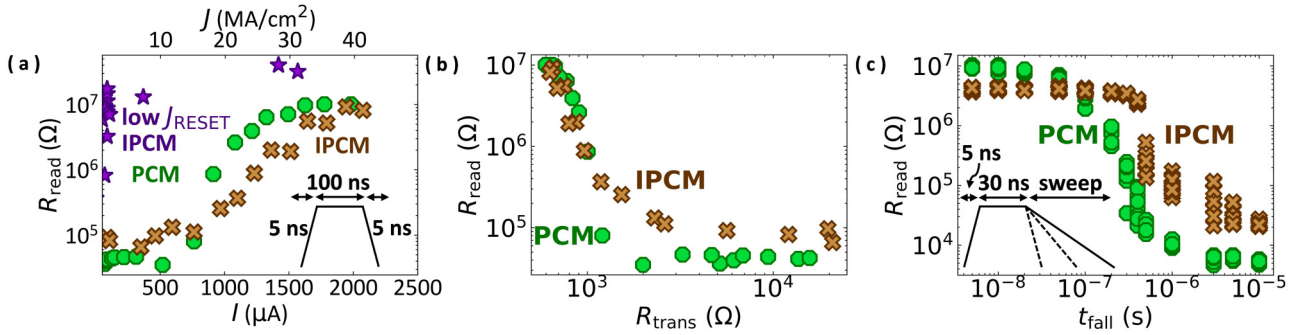

FIG. 3. (a) R_{read} vs I of relatively well-behaved PCM (green) and IPCM (brown). IPCMs with low J_{RESET} currents (purple) were also measured from the same chip (processed through the same run) as the brown device, but they had poor endurance. (b) R_{read} vs R_{trans}. R_{trans} was averaged over the duration of the pulse width (100 ns). Similar trends hint that both PCM and IPCM RESET are based on a melt-quench process. (c) R_{read} vs t_{fall}, indicating both PCM and IPCM RESET by a melt-quench process. The voltage amplitude was fixed at 1.2 V for PCMs and 1.5 V for IPCMs. Ten measurements were performed for each fall time for reproducibility.

unable to perform further measurements, an observation we will return to below. Figure 3(b) shows R_{read} vs R_{trans}, where

$$R_{trans} = \frac{V_{applied} - V_{scope}}{I} \text{ and } I = \frac{V_{scope}}{50\,\Omega}. \quad (1)$$

R_{trans} is the resistance of the device under test (DUT), while the voltage pulse is being applied. For the reference PCM, because the BE diameter is larger than the GST thickness, the entire stack between the top and the bottom electrode gets heated during RESET. Due to the temperature dependence of the electrical resistivity of GST,[45] the resistance of the PCM must go through a low transient resistance state before reaching a higher final DC read resistance state. Interestingly, we find IPCMs following the same trend, suggesting a melt-quench based RESET.

To verify that the low R_{trans} in IPCMs originates from a thermal process rather than from electric fields, pulsed measurements as a function of pulse fall time (t_{fall}) were performed using a fixed voltage amplitude shown in Fig. 3(c). We find both PCM and IPCM R_{read} are dependent on t_{fall} and conclude that both exhibit melt-quench based RESET. Importantly, although the RESET mechanism of IPCMs has been debated, to the best of our knowledge, there have been no experimental demonstrations of nonvolatile DC RESET of IPCMs to date. The one close exception is a demonstration of volatile selectorlike DC RESET.[28] Since a dependence on rapid cooling is the defining characteristic of melt-quench based RESET, we anticipate that if a fundamentally new mechanism exists, it should be possible to demonstrate slow cooling RESET (i.e., DC RESET).

IV. PROCESS ANALYSIS

To gain additional insight, IPCM devices were cross-sectioned and imaged by scanning electron microscopy (SEM). Figure 4(a) shows an example of an as-fabricated device that has not been electrically probed, showing defects including surface roughness and voids within the IPCM layer. The distribution of voids is stochastic, and depending on the specific device and cutting angle, images without voids were also obtainable (example shown in Fig. 5). Figures 4(b) and 4(c) show conceptual diagrams of a possible cause of J_{RESET} reduction when a void is present near the BE. Initially, the void is static because there are no driving forces on the surrounding atoms. Once a voltage pulse is applied across the TE and BE, the current generates a hot spot with a radial temperature gradient above the BE due to Joule heating of the chalcogenide/BE contact. Because hot atoms move much faster than the slow atoms, this causes a net flux of atoms from the hot region toward cold regions with voids. This process can effectively be seen as voids being attracted toward the region above the BE in the presence of a

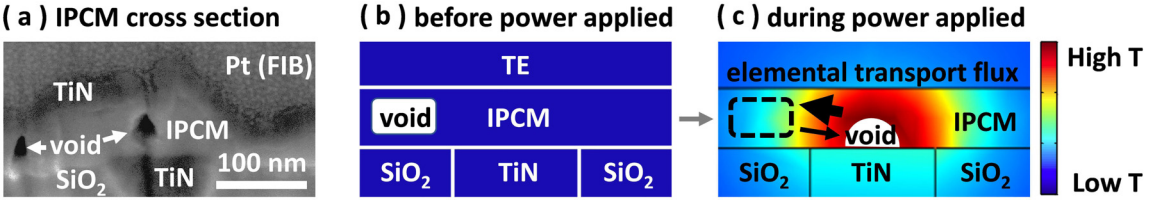

FIG. 4. (a) Cross-sectional SEM of an as-processed IPCM device prior to electrical probing, showing voids within the IPCM. (b) and (c) Conceptual diagrams illustrating possible J_{RESET} reduction mechanism: temperature gradients during RESET cause atomic diffusion from above the BE (hot region) to colder regions with voids (i.e., thermophoresis). Consequently, nearby voids are attracted above the BE, reducing the effective device size, thus reducing the apparent J_{RESET}.

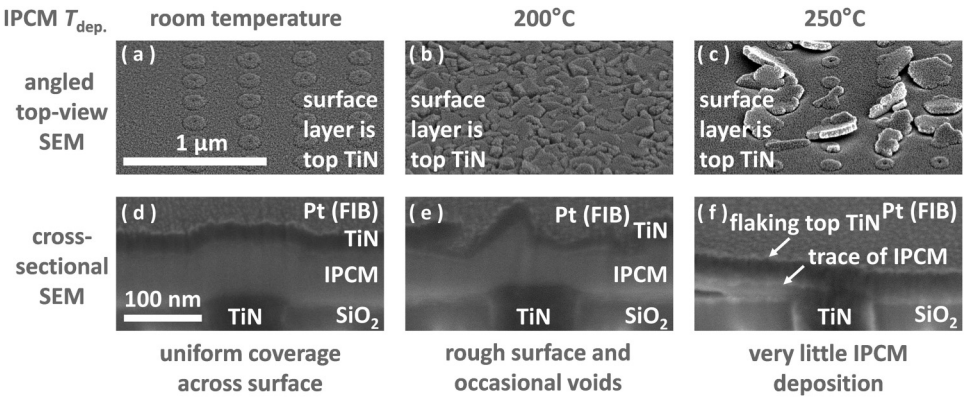

FIG. 5. Morphology of IPCM as a function of deposition temperature. (a)–(c) Top-view SEMs of depositions at room temperature, 200 °C and 250 °C, respectively. (d)–(f) Cross-sectional SEMs of depositions at room temperature, 200 °C and 250 °C, respectively.

temperature gradient (i.e., thermophoresis or thermodiffusion).[47] Since PCMs are not filamentary devices, the RESET current is roughly proportional to the chalcogenide/BE contact area. Hence, once the contact area is reduced by the voids, the RESET current is expected to reduce. This mechanism also explains why we observed significant J_{RESET} variation between IPCM devices. If a void is not present within an accessible range of the temperature gradient, devices RESET in a well-behaved manner at consistent voltages, but with relatively high J_{RESET} due to no IPCM/BE contact area reduction.

Finally, control tests were performed to further understand the dependence of IPCM morphology on deposition temperature. Figure 5 shows top-view and cross-sectional SEMs of TiN/IPCM/BE test structure arrays. The cross-sectional SEMs have an additional Pt layer on the surface deposited *in situ* during FIB sample preparation. When deposited at room temperature, IPCM films were very conformal, with the BE morphology visibly carrying over to the surface. At 200 °C deposition temperature, surface roughness and voids become visible, clearly degrading the integrity of the film. As mentioned previously, the void distribution is stochastic. In contrast to Fig. 4(a), Fig. 5(e) shows an example of a device with no apparent nearby voids. At 250 °C, minimal IPCM deposition is observed, with the TiN TE layer depositing on small IPCM islands on the surface causing flaking. The deposition time of the stack was kept constant for all three films. Similar morphological trends dependent on deposition temperature were observed with GST as well, and are shown in Sec. 8 in the supplementary material. Additional control tests are presented in Sec. 9 in the supplementary material showing thermal instability of solid-phase chalcogenides at elevated temperatures (200–250 °C) due to sublimation, which is likely related to void formation. One possible path toward avoiding these issues may be to deposit IPCMs at room (or lower) temperatures, followed by deposition of a capping layer, and subsequent annealing to prevent sublimation. Prior work has been shown that intermixing of Sb_2Te_3/GeTe becomes problematic at 400 °C annealing,[48] but further investigation remains as future work.

V. CONCLUSION

In summary, the contributions of this work are the following: (1) thermal characterization of IPCM films including period-dependent κ_{eff} (as low as ~0.4 W m^{-1} K^{-1}) and TBR of the Sb_2Te_3/GeTe interface (~3.4 m^2 K GW^{-1}); (2) finite element simulations showing IPCM thermal properties alone cannot account for substantial (~100×) J_{RESET} reductions; (3) electrical measurements showing both PCM and IPCM exhibit melt-quench-based RESET, and pointing out that no prior work has shown nonvolatile DC RESET; (4) discovery of randomly generated voids within chalcogenide films deposited at high (~200 °C) temperatures; (5) proposing an alternate mechanism for the large apparent reduction of J_{RESET} in IPCM based on our findings and well-known physics; (6) control tests showing sublimation of $Ge_2Sb_2Te_5$ and Sb_2Te_3 at elevated (~250 °C) temperatures, possibly related to void formation; and (7) various other supplementary content, including surveys of IPCM RESET current density and selector ON current density.

SUPPLEMENTARY MATERIAL

See the supplementary material for (1) survey of selector ON current densities, (2) survey of IPCM J_{RESET}, (3) PCM and IPCM film deposition conditions, (4) Sb_2Te_3/GeTe thermal boundary resistance extraction, (5) finite element simulation assumptions and methodology, (6) electrical measurement setup, (7) PCM and IPCM cycle-to-cycle RESET variation, (8) morphology of PCM dependent on deposition temperature, (9) control tests with varying postdeposition annealing conditions showing sublimation of Sb_2Te_3 and $Ge_2Sb_2Te_5$, and (10) sputtering chamber cooling and pumping rates.

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Supplementary Material

Understanding the Switching Mechanism of Interfacial Phase Change Memory

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1. Survey of Selector ON Current Densities

Figure S1 shows a survey of ON current densities of selectors. Importantly, most selectors cannot supply high enough ON current densities typically required to RESET PCMs. Selectors shown include volatile conductive bridge random access memory (CBRAM), metal-insulator-metal (MIM) structures with Schottky emission-based conduction, metal-semiconductor-metal (MSM) structures with tunneling based conduction, diodes, insulator-metal-transition (IMT) selectors, Ovonic threshold switches (OTS), and other types of selectors. Other types of selectors include a Pt/TaO_x/TiO_2/TaO_x/Pt multi-layer tunneling barrier selector and a super linear threshold selector with an undisclosed material stack. The selectivity shown in Fig. S1 (a) was defined as J_{ON}/J_{OFF}. J_{ON} was defined as the current density corresponding to the supply voltage (= V_{DD}). J_{OFF} was defined as the current density corresponding to half V_{DD}. For selectors with abrupt switching mechanisms (volatile CBRAM, OTS, IMT), V_{DD} was chosen right after the abrupt switching. For selectors with non-abrupt switching mechanisms (continuous *I-V* characteristics), V_{DD} was taken with discretion, choosing points favoring ON current densities over selectivity. Typical limiting factors of the ON current density include: 1. volatile CBRAM (conducting area) 2. MIM Schottky (barrier height) 3. MSM tunnel (barrier height, barrier thickness) 4. diode (series resistance, space charge limited) 5. OTS (thermal stability to retain high resistance state after self-Joule heating) 6. IMT (material conductivity at metallic state).

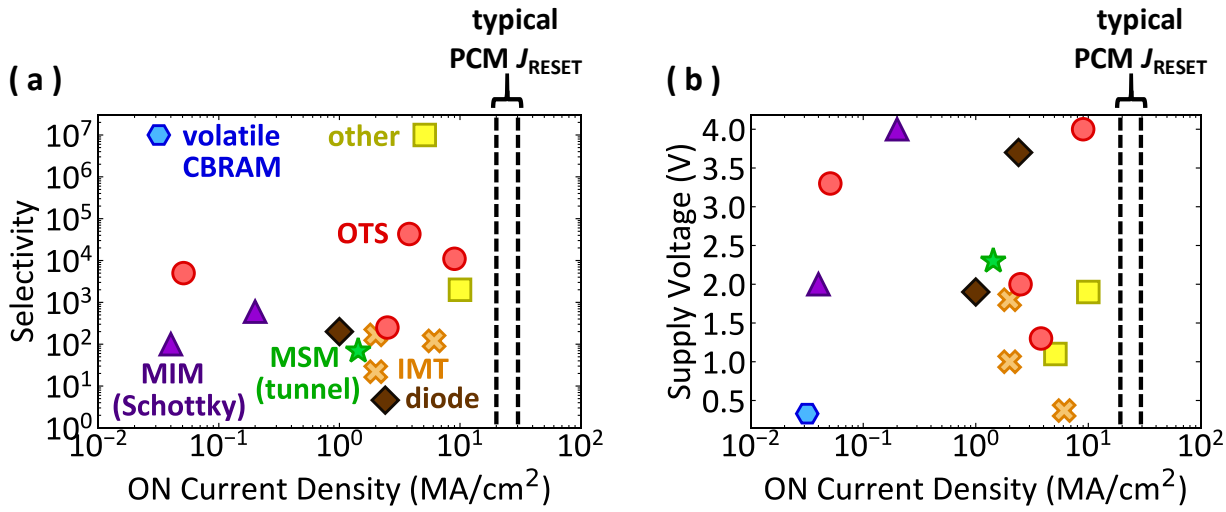

FIG. S1. Survey of ON current densities of selectors compared against (a) selectivity and (b) threshold voltage. References: volatile conductive bridge random-access memory (CBRAM, blue hexagon),[1] Schottky emission based metal-insulator-metal (MIM) structures (indigo triangles),[2,3] tunneling conduction based metal-semiconductor-metal (MSM) structures (green star),[4] insulator-metal transition (IMT, orange cross),[5-7] diode (brown diamonds),[8,9] Ovonic threshold switch (OTS, red circles),[10-13] other types of selectors (yellow squares).[14,15]

2. Survey of IPCM J_{RESET}

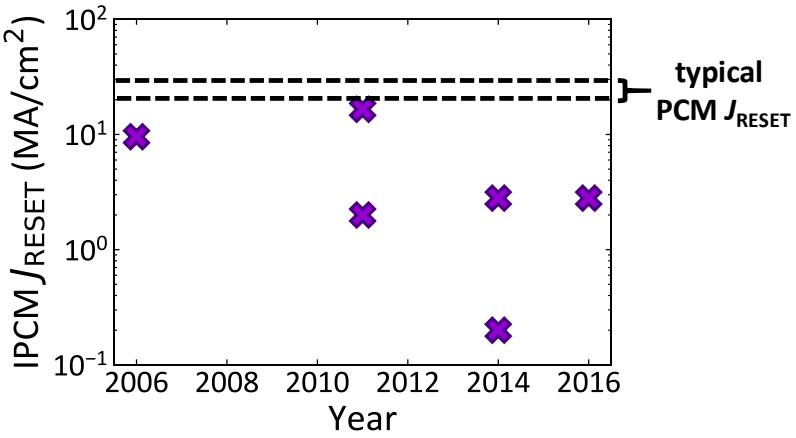

FIG. S2. Survey of IPCM J_{RESET}.[16-21] For papers that provided reference PCM I_{RESET}, but no device dimensions, the IPCM J_{RESET} was estimated assuming PCM J_{RESET} of 20 MA/cm^2.

3. PCM and IPCM Film Deposition Conditions

The switching layer and top electrodes (Sb_2Te_3/GeTe stack, $Ge_2Sb_2Te_5$, TiN, Pt) were deposited using an AJA International Inc. ATC 1800-F sputtering system. The wafer holder and target diameter used are ~4 inches and 2 inches, respectively. The target to substrate distance is ~6 inches. The Sb_2Te_3/GeTe stack and $Ge_2Sb_2Te_5$ layer was deposited at 200°C at 4 mTorr using Ar with 30 W input power unless noted otherwise. Sb_2Te_3, GeTe, and $Ge_2Sb_2Te_5$ compound targets were used (as opposed to co-sputtering single element targets). Prior to IPCM/GST deposition, an Ar plasma etching was performed for 3 minutes at 50 W and 5 mTorr to etch the native oxide surface of the TiN BE. For the devices used for electrical measurements, ~60 nm of TiN and ~100 nm of Pt was deposited after the chamber heater was turned off. The TDTR samples were deposited with the

same conditions described above and were capped with ~80 nm of Al *in situ* (*i.e.* without breaking vacuum) after the IPCM multilayer deposition. The cooling and pumping rates of this chamber is shown in supplementary section 10 for reference.

4. Sb_2Te_3/GeTe Thermal Boundary Resistance Extraction

The thermal resistance of a single period of a [Sb_2Te_3 : GeTe] IPCM stack, R_d, can be expressed as

$$R_d = \frac{d_{Sb_2Te_3} + d_{GeTe}}{\kappa_{eff}} = \frac{d_{Sb_2Te_3}}{\kappa_{Sb_2Te_3}} + \frac{d_{GeTe}}{\kappa_{GeTe}} + 2R_i$$

where R_i is the thermal boundary resistance (TBR) of the Sb_2Te_3/GeTe interface, κ_{eff} is the effective cross-plane thermal conductivity of the IPCM superlattice, $\kappa_{Sb_2Te_3\ (GeTe)}$ and $d_{Sb_2Te_3\ (GeTe)}$ are the thermal conductivity and thickness of the Sb_2Te_3 (GeTe) layer, respectively.
In our samples, we fix $d_{Sb_2Te_3} = 4d/5$ and $d_{GeTe} = d/5$, where d is the IPCM period thickness. Thus,

$$R_d = \frac{d}{\kappa_{eff}} = \left(\frac{0.8}{\kappa_{Sb_2Te_3}} + \frac{0.2}{\kappa_{GeTe}}\right) d + 2R_i$$

Figure S3 [same as Fig. 1(c)] shows the measured thermal resistance R_d vs. d along with a linear fit. The vertical intercept of the linear fit at $d = 0$ represents $2R_i$. The extracted TBR is R_i ~3.4 m^2KGW^{-1}, noticeably lower than prior TBR studies of GST/TiN (~26 m^2KGW^{-1})[22] and GST/SiO_2 interfaces (~28 m^2KGW^{-1}).[23] One reason could be due to intermixing at the Sb_2Te_3/GeTe interface, which may be of interest for future studies. We note that the good linear fit in Fig. S3 suggests no significant quasi-ballistic phonon contribution even in the samples with thinnest period ($d \approx 5$ nm). If this were the case, one would expect to see a deviation from the linear fit for the thinnest periods measured (*i.e.* higher effective thermal resistance).

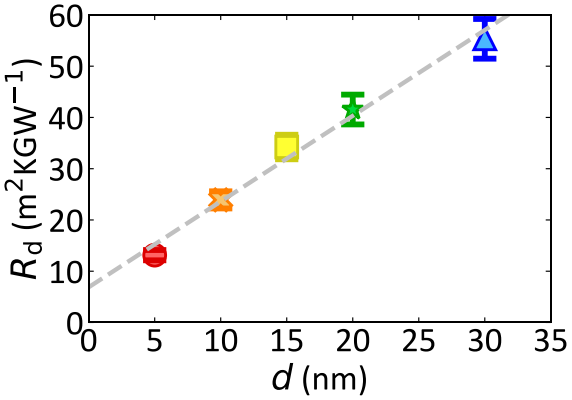

FIG. S3. Measured R_d vs. d and linear fit for TBR extraction of the Sb_2Te_3/GeTe interface. R_d is the thermal resistance of a single period of a [Sb_2Te_3 : GeTe] IPCM stack, and d is the unit period thickness. The relative film thicknesses are fixed to $d_{Sb_2Te_3} = 4d/5$ and $d_{GeTe} = d/5$. The vertical intercept corresponds to $2R_i$.

5. Finite Element Simulation Assumptions and Methodology

COMSOL Multiphysics® 5.2 was used for finite element simulations. The model was built with materials and geometric structures shown in Fig. 2 (a), with axisymmetry about the y axis. For the (I)PCM switching layer material properties, we made the following assumptions:

1) Temperature dependent bulk electrical resistivity, ρ_b (T), of GST,[24] with $\rho_b = 9.39\times10^{-6}$ Ωm above 930 K.

2) $\kappa_{eff}(T) = \alpha\,\kappa_{GST}(T)$, where α is the scaling factor we vary and $\kappa_{GST}(T)$ is the temperature dependent thermal conductivity of GST.[25]

For the (I)PCM/BE interface, we made the following assumptions:

1) $\rho_c(T) = t_{eff} \cdot \rho_b(T)$, where $\rho_c(T)$ is the temperature dependent electrical contact resistivity of GST and t_{eff} is a scaling factor we used to convert bulk resistivity to contact resistivity. t_{eff} = 10 nm was chosen which gives reasonable agreement with previously extracted GST/metal contact resistances at room temperature.[26]
2) Temperature dependent thermal boundary resistances, $R_i(T)$, of previously measured GST/TiN interface,[22] with R_i = 18.37 m^2KGW^{-1} above 597 K.

A 180 Ω series resistance was added to the outer edge of the bottom electrode interconnect which takes into account the interconnect resistance. This resistance was determined by fabricating and measuring dedicated test structure chips using identical electrodes we used for electrical measurements. The series resistance plays a role as a thermal runaway limiter by dynamically reallocating the potential distribution across the device as the bulk GST and GST/TiN interface transient resistance decreases and approaches comparable values to that of the series resistance of the interconnects during RESET operation. Joule heating (or resistive loss) at the GST, GST/TiN interface, and electrodes were enabled. The temperature of the heat transfer in the structure was coupled to the temperature dependence when calculating the electric current densities throughout the structure. The boundary of the structure was set thermally and electrically insulated. The model was made sufficiently large (10 µm diameter, 10 µm thickness) to ensure a large thermal capacitance for heat transfer modeling. The latent heat associated with the phase transition was assumed to be negligible compared to the heat generated by Joule heating of bulk GST and contacts of the GST and GST/TiN interface.[27,28] Thermoelectric effects were also assumed to be negligible and not incorporated. A positive voltage pulse was applied to the top electrode. Temperature profiles were captured at 100 ns after applying the voltage pulse. The amplitude of the voltage pulse was increased until a small region of the GST layer exceeded 600°C above room temperature, which was deemed as the "knee" of the *R-I* RESET curve. Multiple cycles of simulations were run with varying κ_{eff} of the GST layer to establish the κ_{eff} dependence of J_{RESET}.

6. Electrical Measurement Setup

The electrical setup used for RF pulsed measurements (*R-I* and fall time dependence) is shown in Fig. S4. A Keysight Technologies B1500A and Agilent Technologies 81160A Pulse Function Arbitrary Generator was connected to a Keithley Instruments 707B switching matrix with a 7173-50 two-pole high frequency matrix card, suited for RF pulsed measurements. The B1500A was used for measuring R_{read}, and the 81160A was used for pulsing. An Agilent Technologies MSO7104A oscilloscope was used with 50 Ω of termination to measure transient currents and transient resistances of the device under test (DUT). We note that while the 1 MΩ termination option available in the MSO7104A may seem better suited for measuring low currents, in practice it is much harder to determine accurate current levels due to a 14 pF capacitance connected in parallel internally within the scope, causing the (DC value) 1 MΩ termination impedance being frequency dependent, as opposed to the purely resistive 50 Ω option which is independent of the frequency. We used a dedicated trigger channel (rather than self-triggering, in which the signal of interest also acts as the trigger signal) to ensure trigger signal levels would always be sufficiently high, regardless of the DUT resistance and DUT channel input voltage level. The voltage resolution of the scope across the 50 Ω termination (~ few mV) ultimately limits our current resolution measurement capability to ~ tens of µA. Devices were tested on a Cascade Microtech Summit 12000 semi-automatic probe station. All electrical measurements were computer controlled with Python programs interfaced via PyVISA.

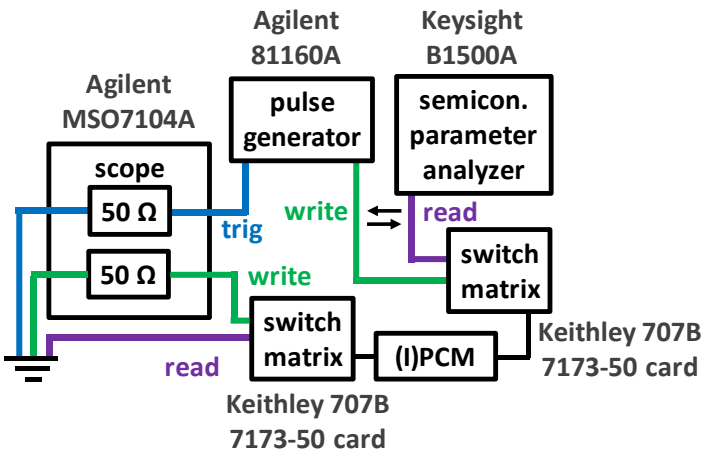

FIG. S4. Electrical equipment setup used for pulsed (I)PCM measurements.

7. PCM and IPCM Cycle-to-Cycle RESET Variation

The cycle-to-cycle variation of well-behaved PCM and IPCM devices are shown in Fig. S5. The larger cycle-to-cycle variation seen in IPCM could be due to a number of factors including microscopic void movements, void coalescence within the film, intermixing of the Sb_2Te_3/GeTe interface, and/or elemental migration of atoms during RESET. Both PCM and IPCM were deposited at 200°C. If higher void densities are involved in causing higher cycle-to-cycle variations, this could imply that Sb_2Te_3 and/or GeTe favor transitioning into gas phases at lower temperatures compared to $Ge_2Sb_2Te_5$ (Fig. S7).

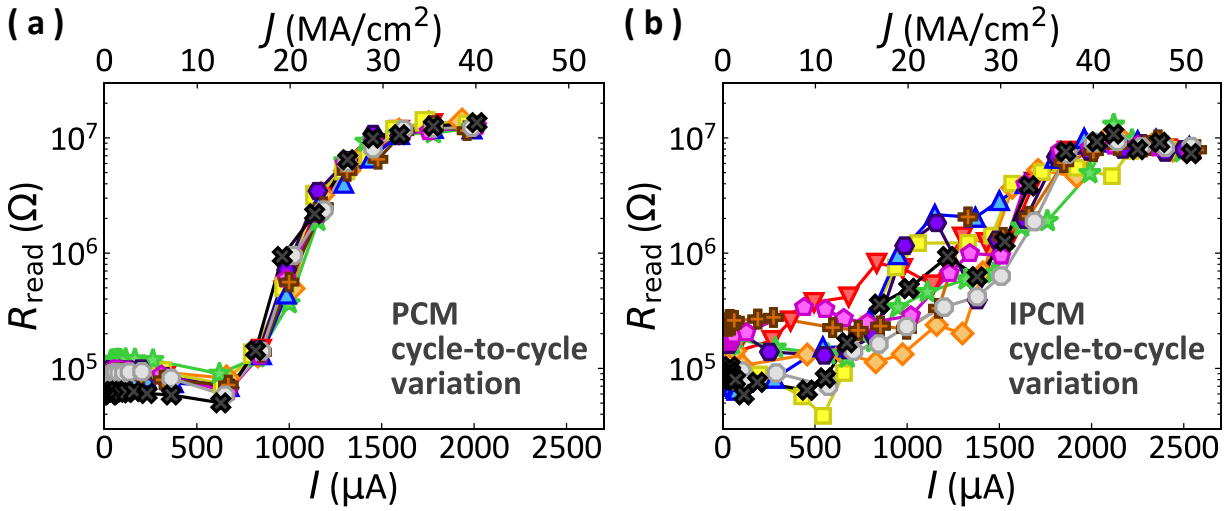

FIG. S5. (a) PCM and (b) IPCM cycle-to-cycle RESET variation

8. Deposition Temperature Dependent Morphology of PCM

Figure S6 shows deposition temperature dependent top-view and cross-sectional SEM images of TiN (TE)/PCM/TiN (BE) memory arrays. The deposition time of the GST and TiN films were kept constant when varying the deposition temperature. Samples using heated deposition were simultaneously cooled and pumped immediately following deposition. The sputtering chamber cooling and pumping rates are shown in supplementary section 10 for reference. The cross-sectional SEMs have an additional Pt layer on the surface deposited *in situ* during FIB sample preparation. The GST morphology trends are similar to that of IPCMs shown in the main text; depositions are conformal at room temperature. Surface roughness and voids appear

within the PCM layer at 200°C. Reduced deposition rates are observed at 250°C. As we discuss in the following section, the apparent reduction in deposition rates are attributed to increasing sublimation rates at higher temperatures. Interestingly, we observe that the $Ge_2Sb_2Te_5$ thickness above the TiN region is thicker than that of the SiO_2 region, suggesting substrate materials may play a role in sublimation rates.

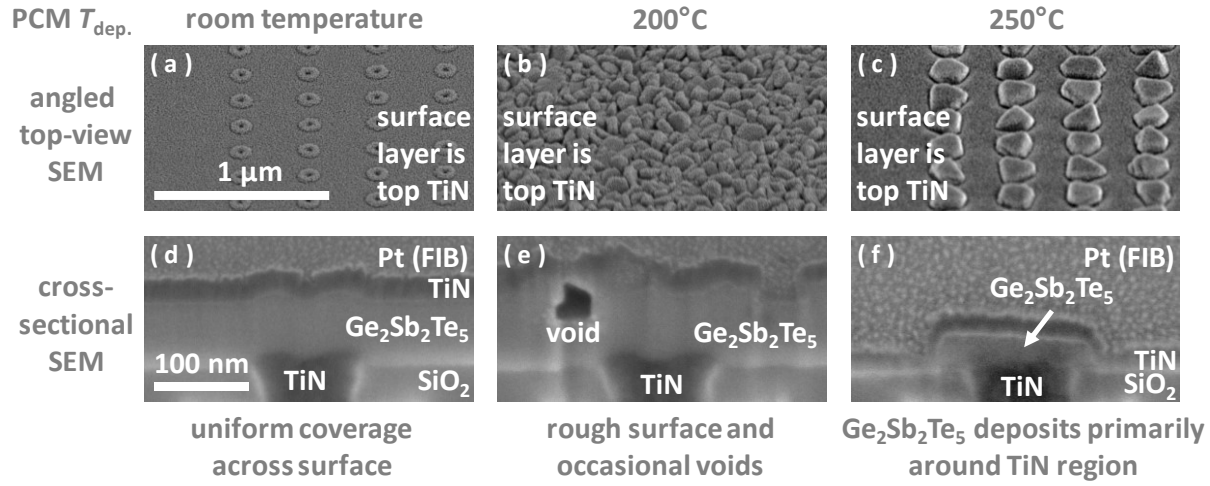

FIG. S6. Deposition temperature dependent morphology of PCM.

9. Control tests with varying post-deposition conditions showing sublimation

In this section, we examine a possible cause of voids and surface roughness observable at elevated deposition temperatures. Figure S7 shows the vapor pressure diagram of the single elements composing PCM and IPCM, namely, Ge, Sb, and Te.[29, 30] In particular, Te is most vulnerable to sublimation when the temperature is increased. Control tests were performed on Sb_2Te_3 and $Ge_2Sb_2Te_5$ to examine whether sublimation of compounds including Te can inherently be problematic at high deposition temperature conditions (200~250°C). Figure S8 show top-view and cross-sectional SEM images of Sb_2Te_3 and $Ge_2Sb_2Te_5$. Sample (a) and (c) were deposited at *identical* conditions (200°C, 4 mTorr in Ar ambient), but with different *post*-deposition conditions. Sample (b) and (d) were similarly deposited with identical conditions with varying post-deposition conditions. Samples (a) and (b) were cooled immediately following Sb_2Te_3 (or $Ge_2Sb_2Te_5$) deposition with a constant 4 mTorr pressure in Ar ambient, followed by TiN TE deposition and pumping of the chamber prior to sample extraction. On the other hand, samples (c) and (d) were annealed an additional 24 hours at 4 mTorr in Ar ambient after Sb_2Te_3 (or $Ge_2Sb_2Te_5$) deposition. The samples were subsequently cooled with a constant 4 mTorr pressure Ar ambient, followed by TiN TE deposition and chamber pumping prior to sample extraction. If no significant sublimation was playing a role at these chamber conditions, one should expect roughly equal chalcogenide film thicknesses. However, as seen in Fig. S8, hardly any Sb_2Te_3 or $Ge_2Sb_2Te_5$ was observable after additional annealing, indicating sublimation. Voids observable in the samples without additional annealing could possibly be related to sublimation, but with weaker effects. From a practical perspective, in order to utilize voids for RESET current and power reduction, precise void size and placement control will likely be crucial to minimize device-to-device variability, and significant process techniques and/or enhancements will be required. Moreover, whether such devices will be able to operate reliably (stable operating voltages, decent retention, high endurance etc.) remains questionable.

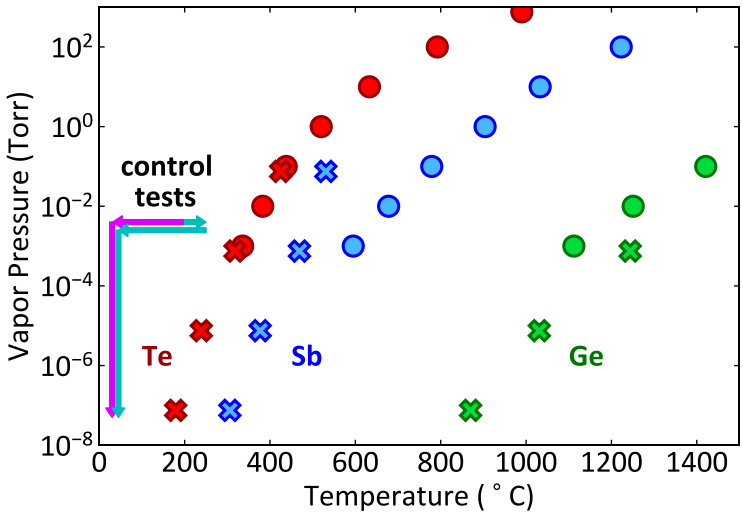

FIG. S7. The vapor pressure diagram of single elements composing $Ge_2Sb_2Te_5$ and the post-deposition temperature-pressure path followed in control tests for Fig. S8. Data points shown in × and ○ are adapted from references 29 and 30, respectively.

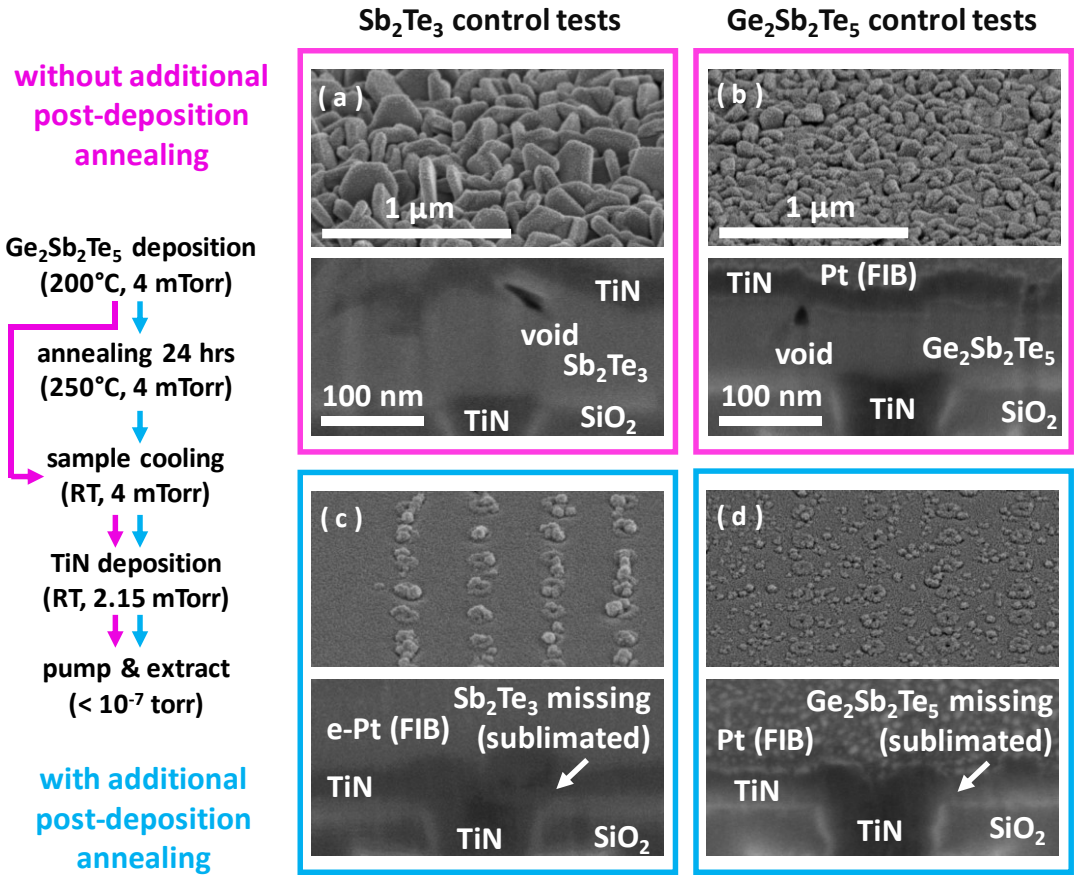

FIG. S8. Control tests with varying post-deposition conditions for (a, c) Sb_2Te_3 and (b, d) $Ge_2Sb_2Te_5$. Additional annealing at 4.0 mTorr, 250°C causes sublimation of the chalcogenides.

10. Sputtering Chamber Cooling and Pumping Rates

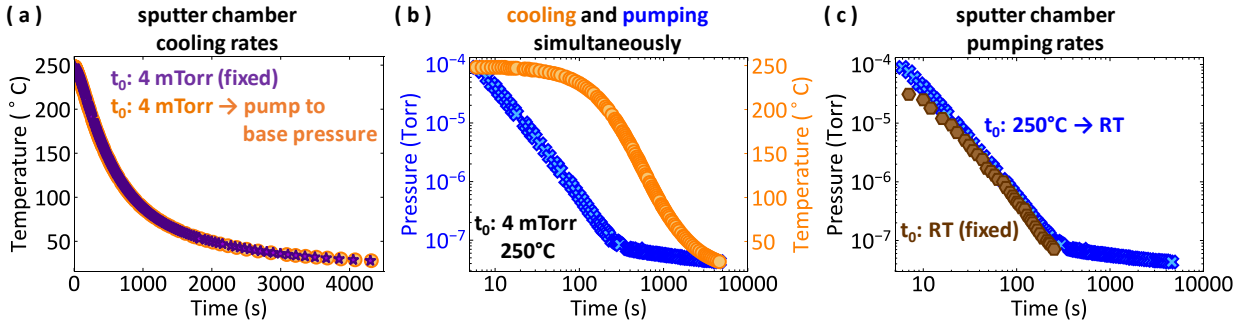

FIG. S9. Sputter chamber cooling and pumping rates. (a) Cooling rate of sputter chamber with (orange circle) and without (purple star) pumping. (b) Cooling (orange circle) and pumping (blue cross) rates when simultaneously cooling and pumping the chamber. (c) Pumping rate of sputter chamber with (blue cross) and without (brown octagon) initial heating conditions. The orange circle in (a) and (b) as well as the blue cross in (b) and (c) are from the same measurement and are shown for reference.

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