Dual-Layer Dielectric Stack for Thermally Isolated Low-Energy Phase-Change Memory

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***Abstract*— High reset energy is an ongoing issue for phase-change memory (PCM) devices. Prior work demonstrates that smaller PCM switching volume and thermal isolation can reduce the reset energy. In this paper, we fabricate and measure a planar confined PCM device with a multilayer dual-layer stack (DLS) of SiO_2/Al_2O_3 insulator. Devices with contact area of 500 × 20 nm and lengths of 2 µm show exceptionally low reset energies of 18.25 ± 15.8 pJ and low reset current densities of 0.94 ± 0.51 MA/cm^2. Implementing the DLS enables a 60% reduction in reset energy compared with SiO_2-isolated devices.**

***Index Terms*— Phase-change memory (PCM), reset energy, thermal conductivity, thermal design.**

I. Introduction

PHASE-CHANGE memory (PCM) has reached production as a nonvolatile storage-class memory (SCM), with access times and costs between NAND flash and DRAM [1]–[3]. In order to create high-density SCM, lower reset energy PCM is required. The high reset energy stems from the temperatures (between 800–1000 K) required to heat and melt the phase-change layer [1]. Two main techniques have been implemented toward lowering the reset energy: reducing the phase-change volume melted via device size scaling [4]–[8] and cell design [9]–[12] or achieving better heat confinement in the structure to create higher temperatures for an applied energy [13]–[15]. To reduce the volume melted, small contact areas have been implemented, down to two nm via carbon nanotube contacts, lowering the reset energy to ∼1 pJ [5]–[7]. In addition, unique cell designs, such as mushroom [8], edge [9], [10], and confined [11] structures have been implemented to limit the phase-change volume melted. Several works investigated the thermal confinement of the mushroom type structure by implementing thermally resistive bottom electrodes. TiN/TaN multilayers [13], fullerenes [14], and graphene bottom electrodes [15] were used and show 90% power reduction, 75% current reduction, and 40% current reduction compared with control devices with standard electrodes, respectively. For confined and edge structures, the relative heat loss through the surrounding insulators is significantly higher. Specifically, for confined cells as shown in Fig. 1(a), thermal simulations show that 89% of the heat is dissipated into the insulator [16]. A strong reduction of the reset energy is predicted by reducing the thermal conductivity of the insulator [16], [17].

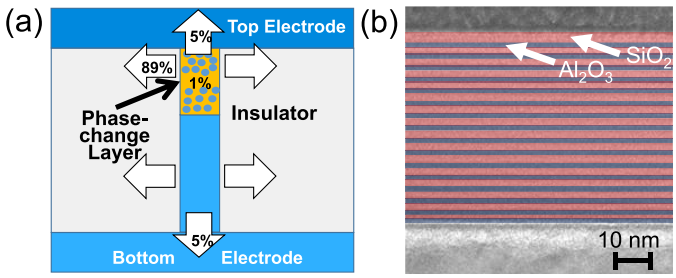

Fig. 1. (a) Schematic of confined cell device structure used for low-power PCM [11]. Arrows represent heat loss paths and energy stored in the phase-change layer during heating. Adapted from [16]. (b) False-colored TEM of the SiO_2/Al_2O_3 multilayer insulator. This film exhibits lower thermal conductivity compared with SiO_2 [16]. This paper implements the multilayer insulator into a planar confined cell to reduce insulator heat loss.

In this paper, we implement an SiO_2/Al_2O_3 multilayer [16], [17] for the insulator of a planar confined PCM device. A false-colored TEM of the multilayer SiO_2/Al_2O_3 dual-layer stack (DLS) is shown in Fig. 1(b). Devices using the DLS as the insulator require ∼60% less reset energy than devices with SiO_2. Scanning thermal microscopy (SThM) and Raman mapping are used to identify the highest temperature region and thus the phase-transformation region: the interface between the phase-change layer and the patterned electrode. Scaling the phase-change volume (via length scaling) reduces the energy, implying that the bulk region is where most of the energy is generated during switching. The fabrication process flow and a further description of the multilayer SiO_2/Al_2O_3 are described in Section II. Section III describes how the various device electrical measurements were conducted. Specifically, the following data will be presented: DC sweep response,

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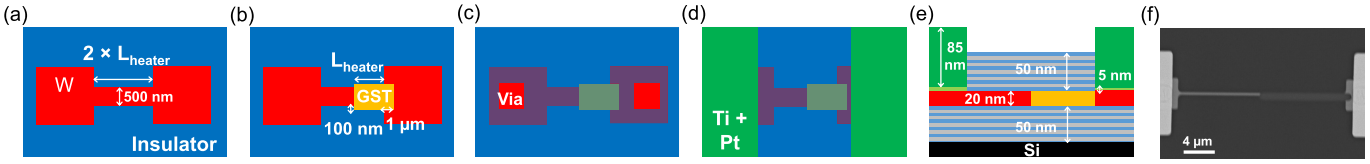

Fig. 2. (a)–(d) Process flow to fabricate planar confined PCM devices (top view). (a) First, an insulator blanket layer of either SiO_2 or DLS was deposited. Then, W was e-beam evaporated. The W was then patterned to form pads and lines, while the remaining area was dry-etched. (b) Phase-change region was patterned, then W was dry-etched, and then a GST layer was deposited and lifted-off. This created a self-aligned GST region. (c) Top insulator blanket layer was deposited with the same film as the bottom layer. The insulator layer was then patterned and wet-etched to form vias to contact the pads. (d) Large pads were then patterned. Ti + Pt was deposited to form the pads and contact the PCM device. (e) Side profile view of the final fabricated structure. (f) SEM of the final fabricated device (top view).

resistance transition due to applied current, endurance, and reset energy for different device dimensions. In Section IV, SThM measurements will be used to identify the location of the switching region and finite-element (FE) simulations and analytical models will be used to describe the heat generation through the PCM device.

II. Fabrication Process Flow and Dielectric Stack

The planar confined PCM devices were fabricated using the process flow outlined in Fig. 2. First, the bottom insulator layer was deposited onto Si wafers. The samples were split between control films, which had 50 nm of plasma-enhanced chemical vapor deposition (PECVD) SiO_2, and DLS films, which had an atomic layer deposition (ALD) oxide comprising of $[SiO_2\ (2)/Al_2O_3\ (1)]_{17}$ multilayer (where $[SiO_2\ (A)/Al_2O_3\ (B)]_C$ means A-nm thick SiO_2 layers and B-nm thick Al_2O_3 layers repeated C times). The ALD SiO_2 and Al_2O_3 were deposited using O_2 plasma with Tris[dimethylamino]silane for SiO_2 and Trimethylaluminum for Al_2O_3 deposition. Next, a 20-nm W layer was deposited using e-beam evaporation. The W layer was then patterned and dry-etched with SF_6 [20] to form the electrode pads and metal line. For the W line, the width remaining was 500 nm and the length was varied to 4, 10, and 20 µm. Next, half of the metal region was patterned to form the phase-change region. The width for this pattern was 500 + 100 nm overshoot on each edge (to account for misalignment to the W metal line) and the length was half of the W line length +1 µm into the pad. This patterned region was then etched to remove all of the W and filled with 20 nm of sputtered $Ge_2Sb_2Te_5$ (GST). The remaining GST on the unpatterned regions was then lifted off to create the self-aligned phase-change layer seen in Fig. 2(b). Following lift-off, the entire wafer was coated with a top insulator. The SiO_2 control samples were formed by depositing 10 nm of ALD SiO_2 + 40 nm of PECVD SiO_2. The DLS samples were formed by ALD depositing $[SiO_2\ (2)/Al_2O_3\ (1)]_{17}$. After the top insulator was deposited, via holes were patterned and wet-etched with 20:1 buffered oxide etch to contact the metal pads. Finally, 5-nm Ti + 85-nm Pt pads were patterned, deposited by e-beam evaporation, and lifted off. The final structure is shown via scanning electron microscope (SEM) in Fig. 2(f).

The multilayer DLS film comprising of $[SiO_2\ (2)/Al_2O_3\ (1)]$ repeated shows low thermal conductivity and was developed

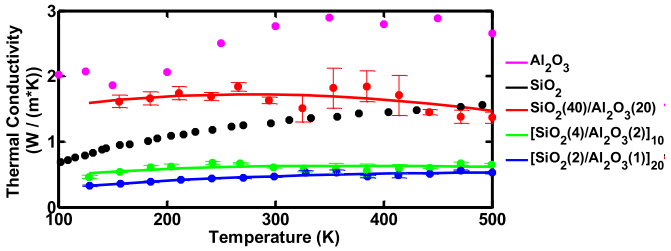

Fig. 3. Through-plane thermal conductivity of SiO_2/Al_2O_3 multilayers with 60-nm total thickness and varying individual layer thicknesses ($[SiO_2\ (A)/Al_2O_3\ (B)]_C$ means A-nm thick SiO_2 layers and B-nm thick Al_2O_3 layers repeated C times). The thermal conductivity decreases as the layer thickness decreases [16]. The multilayer films exhibit lower thermal conductivity than their bulk ALD SiO_2 [18] and Al_2O_3 [19] constituents.

in previous work [16]. The through-plane thermal conductivity of this film was measured using a steady-state electrothermal measurement of a metal heater on the film [16]. By measuring the change in electrical resistance of the metal heater due to applied power and at different temperatures, the thermal resistance of the multilayer film was extracted [16], [21]. Then, assuming 1-D heat conduction through the film, an effective thermal conductivity was calculated. Samples with various number of layers with the same total thickness (60 nm) were deposited, and the resulting thermal conductivities are shown in Fig. 3. The thermal conductivity of the DLS film is significantly lower than bulk ALD SiO_2 [18] and Al_2O_3 [19] films. Increasing the number of layers reduces the thermal conductivity, ultimately reaching a 64% reduction when compared with the bulk SiO_2 thermal conductivity. The decrease in thermal conductivity is attributed to two main reasons: a change in film quality resulting in lower density and thus lower intrinsic thermal conductivity of each of the layers, and a finite thermal boundary resistance (TBR) between the two layers of $\sim$1.5 m^2K/GW, which contributes significantly when the number of layers is large [16]. This multilayer film was leveraged to create a thermally confined PCM device [17] and is further explored in this paper.

III. Electrical Measurements

Electrical resistance measurements of the devices were performed using an HP 4156C Parameter Analyzer, programming pulses were applied via an Agilent 811110A pulse generator, and a 707B Keithley switch matrix was used

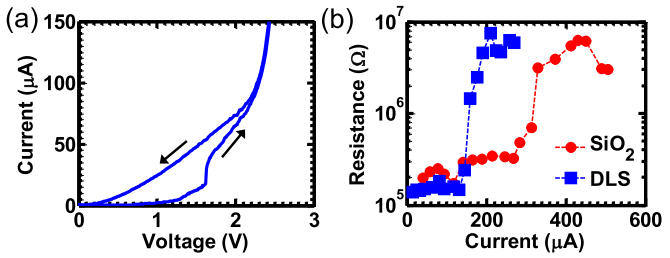

Fig. 4. For a typical $L_{heater} = 10\ \mu$m device. (a) *I–V* curve obtained from a DC voltage sweep of a SiO_2-insulated device. The device starts in the reset (high resistance) state and undergoes threshold switching. The device's resistance is then set to the low resistance state as the DC sweep returns. (b) *R–I* plot of the SiO_2 and DLS-insulated device's response to reset pulses with various voltages. The voltages applied are increased in 0.5-V steps. The resulting current increases, resulting in larger energies generated in the PCM device. The devices switch to the reset state once a large enough energy is applied. The SiO_2 devices switch with $341 \pm 27\ \mu$A, while the DLS devices switch with $190 \pm 13\ \mu$A (25 measurements on the same device).

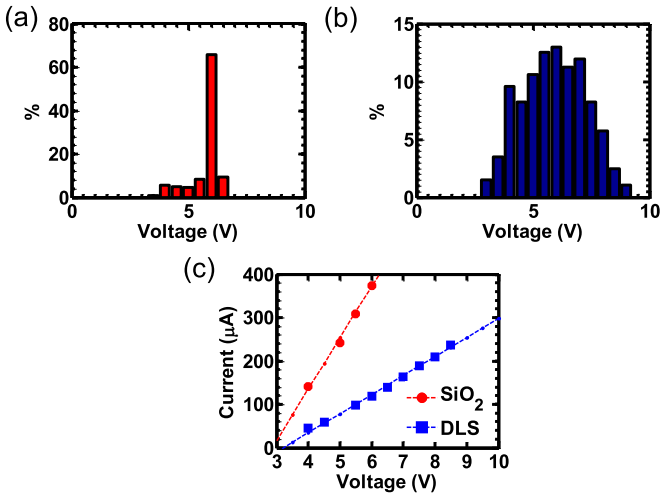

Fig. 5. For a typical $L_{heater} = 5\ \mu$m device. (a)and (b) Histogram distribution of the voltages required to reset the (a) SiO_2 and (b) DLS device. Steps of 0.5 V were taken using the write-verify process until the device showed resistance $> R_{reset}$. (c) Plot of the measured currents to reset a device at their associated reset voltages. 25 measurements each were taken for DLS and SiO_2 devices. The current variation at a given reset voltage was $< \pm 5\%$.

to switch between the two tools. A 200-mV DC voltage was used to read the resistance of the device. Reset and Set were performed by applying a 5/50/5 and 100/1000/100 ns rise/width/fall time pulse, respectively. During programming, the input impedance of a Tektronix DPO4045 Oscilliscope was used as a 50-Ω resistor to ground to measure the current. For all of the following measurements, the devices were first cycled ~1000 times before the actual measurements to prevent any anomalous effects associated with early cycle switching, such as phase-segregation [22].

Several electrical measurements were performed, including a DC voltage sweep to set the devices, an *R–I* curve showing the resistance and currents measured after applying different voltages, from which the average reset energy was derived. First, the DC sweep was measured to identify the threshold switching voltage. Fig. 4(a) shows an example of the DC sweep performed on the $L_{heater} = 10\ \mu$m. The devices showed a threshold voltage between 1 and 2 V. Next, pulsed measurements were performed via gradually increasing voltages, with 0.5 or 0.2 V steps for reset and set. As the voltage pulses were applied, the current during each pulse, I_{reset}, was determined using the following equation:

$$I_{reset} = \frac{1}{t_{pulse}} \int \frac{V_{osc}(t)}{50\Omega} dt \tag{1}$$

where $V_{osc}(t)$ was the measured voltage across the 50-Ω oscilloscope resistor as a function of time and t_{pulse} is the total time the pulse was applied at its maximum value. For the 5/50/5 ns rise/width/fall time pulse, 55 ns was used since 1/2 × [5-ns rise + 5-ns fall] + 50 ns pulsewidth = 55 ns. Fig. 4(b) shows an example of the resulting currents and DC resistance after pulses were applied on the $L_{heater} = 10\ \mu$m devices. The devices were initially in the set state ($R_{set} \leq 200\ k\Omega$) and switch to the reset state ($R_{reset} \geq 2\ M\Omega$) after undergoing the voltage pulses. The $L_{heater} = 2, 5, 10\ \mu$m DLS devices switch at 94 ± 51, 129 ± 62, and 190 ± 13 μA, while the SiO_2 devices switch at 240 ± 83, 329 ± 70, 341 ± 27 μA, respectively (25 measurements on a single devices for each length). The $L_{heater} = 2\ \mu$m DLS devices were thus able to show current densities of 0.94 ± 0.51 MA/cm^2.

A write-verify process was used to cycle the devices and identify the reset energy. In order to perform the process, a 2-V reset pulse is first applied. After the reset pulse, the device resistance is measured. If the resistance measured is below the R_{reset} threshold, then another reset pulse is applied, increasing the previous voltage by 0.5-V increments. The reset pulses are increase until the resistance is above the R_{reset} threshold. Then, set pulses are applied in a similar manner with 0.8-V starting set voltage and 0.2-V steps until the resistance measured is below the R_{set} threshold. The process was repeated to cycle the device. Fig. 5(a) and (b) shows the required voltage measured to reset $L_{heater} = 5\ \mu$m SiO_2 and DLS devices. The current driven at reset was measured 25 times randomly selected from 1000 cycles for each of the device dimensions. An example plot of the measured currents and voltages during reset for the $L_{heater} = 5\ \mu$m DLS and SiO_2 devices is shown in Fig. 5(c). There is a strong linear correlation between the reset voltage, V_{reset}, and current, I_{reset}. Thus, the reset current can be written as a function of the reset voltage, $I_{reset}(V_{reset})$.In addition, for a given reset voltage, the current driven does not change significantly between cycles. The variation in reset current is mostly due to the variation in the required voltage to reset. The energy required to reset PCM devices can thus be estimating using

$$E_{reset} = V_{reset} \times I_{reset}(V_{reset}) \times t_{pulse}. \tag{2}$$

The reset energy was measured for DLS and SiO_2 samples with $L_{heater} = 2, 5$, and 10 μm and is shown in Fig. 6. The DLS devices require ~60% lower energies to switch compared with the SiO_2-isolated devices at all dimensions. In addition, the reset energy decreases with the overall length of the device with the $L_{heater} = 2\ \mu$m devices showing 18.25 ± 15.8 pJ switching energies. The devices were also cycled for endurance testing using the write-verify process.

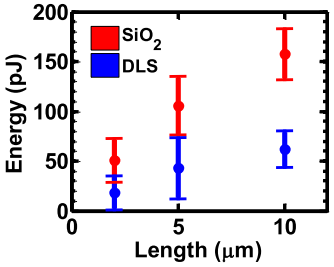

Fig. 6. Energy required to reset devices with different L_{heater} length for SiO_2 and DLS devices. The energy was determined using (2). The DLS devices required ~60% less energy to reset than the SiO_2 devices at all lengths. Decreasing the length shows a decrease in reset energy which implies that most of the reset energy is consumed in the bulk volume of the phase-change layer and not at the interface.

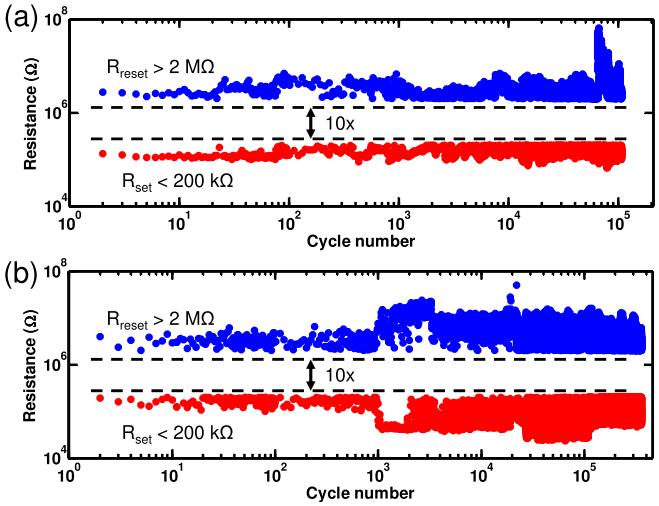

Fig. 7. Measured endurance of $L_{heater} = 10\ \mu m$ (a) SiO_2 and (b) DLS PCM devices. A write-verify process was used. Devices with all different L_{heater} dimensions were able to maintain 10× resistance window for $> 10^5$ cycles.

Devices for all dimensions showed $> 10^5$ endurance cycles. Fig. 7 shows the endurances measured for the SiO_2 and DLS $L_{heater} = 10$ μm devices.

IV. SThM Measurements, FE Simulations, and Analysis

To better understand the power dissipation in the device, the temperature distribution was measured using SThM [23] and Raman thermometry [24], [25]. A commercial SThM module by Anasys Instruments was added onto an atomic force microscope (AFM) from Veeco Instruments. A Horiba LabRam instrument with a 633-nm laser was used for a Raman thermometry following the procedure outlined in [24]. The SThM enables high (AFM-based) spatial resolution, but measures the temperature at the top surface of the insulator layer. On the other hand, Raman directly measures heating in the GST film, but is limited by diffraction to a spatial resolution of ~0.5 μm. The SThM measurement is used to identify the relative temperature profile, while the Raman measurement is used to identify the temperature at the GST layer and hence calibrate the SThM measurement.

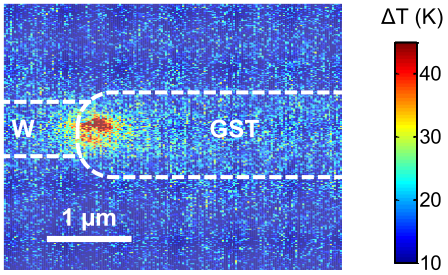

Fig. 8. SThM image of DLS PCM device ($W_{heater} = 1\ \mu m$ and $L_{heater} = 5\ \mu m$) showing the temperature rise under electrical bias ($V = 3$ V and $I \approx 200\ \mu A$ DC during SThM surface temperature mapping) [23]. The temperature was calibrated by a Raman thermometry [24]. The GST channel and W electrode boundaries (dashed white lines) are visible in an AFM topography image acquired simultaneously with the SThM map. The temperature profile shows significant heating at the W/GST contact interface and moderate heating in the bulk GST.

Fig. 8 shows the spatial distribution of the temperature rise for a DLS PCM device ($W_{heater} = 1$ μm and $L_{heater} = 5$ μm). The AFM topography map acquired simultaneously determines the exact position of the GST channel and the electrodes (marked with white dashed lines). Evidently, the highest temperature region is locally at the W/GST contact with some temperature change also generated throughout the bulk GST channel. This implies that the phase-change switching region is near the interface, since that is the highest temperature region. In addition, the finite temperature change along the bulk GST implies that significant power is consumed along the bulk GST to heat up the entire region. Since the bulk volume is much larger than the interfacial switching region, significant power is required to reach even a small temperature change of the bulk GST.

2-D FE simulations were performed to better understand the heating and improvement from using the DLS film. The following Fourier heat diffusion equations with TBRs were used to simulate the steady-state heat flow:

$$\nabla \cdot (k \nabla T) + Q_{heat} = 0 \tag{3}$$

$$Q'' = \frac{\Delta T}{\text{TBR}} \tag{4}$$

where (3) was solved at each node with the following node parameters: k is the thermal conductivity, T is the temperature, and Q_{heat} is the heat generated. For the W/GST interface, Q'' was the heat flux across the interface and had a TBR of 24 m^2K/GW [26]. Fig. 9(a) outlines all boundary conditions used for the simulation. The W and GST contacts with the pad region and Si wafer were assumed to be isothermal, since they act as a heat sink/reservoir, with volumes much larger than the regions simulated. The thermal conductivities used were identical to previous work [16], except for the insulator. The insulator thermal conductivities were selected to match their high temperature values of 1.6 and 0.48 W/(m × K) for SiO_2 and DLS films, respectively [16].

Joule heating was assumed to be the primary heat source for this simulation. Thus, the heat generated could be broken up into two different heating types based on the most electrically resistive locations: 1) the heat generated at the interface to

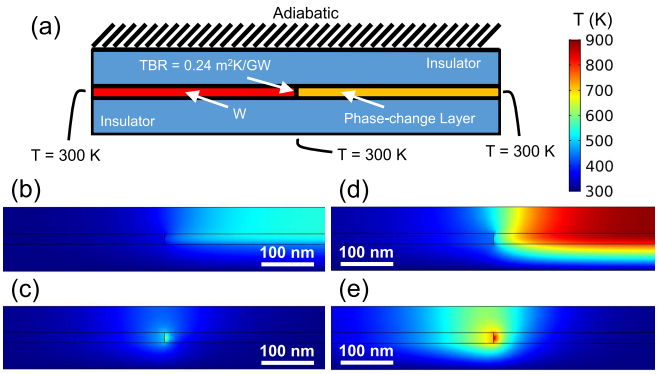

Fig. 9. 2-D FE thermal simulation. (a) Simulation boundary conditions and temperature legend. (b)–(e) Resulting simulation temperature profiles. Simulations compared (b) and (c) SiO_2 devices and (d) and (e) DLS devices. Devices with different L_{heater} lengths were simulated, and the normalized temperature profile near the GST/W interface appeared the same, since the heat transfer length is much shorter than the bulk GST and W length. (b) and (d) Simulations assuming all heat generated in the bulk GST. For the same power, that DLS devices generate 2.4× the temperature change of SiO_2 devices. (c) and (e) Simulations assuming all heat generated at the GST/W interface. For this case, heating of the interface showed 1.6× the temperature change in DLS devices compared with SiO_2 devices.

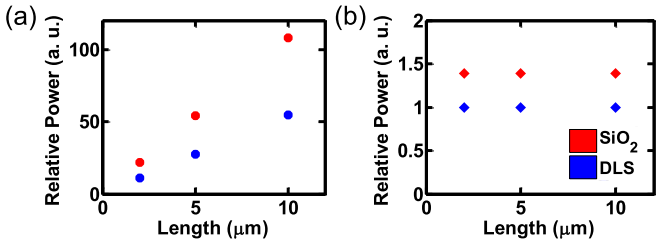

Fig. 10. Simulated reset power required to reach a temperature of 900 K for the different L_{heater} length PCM devices assuming (a) bulk heating and (b) interface heating. The power was normalized to the power required to reach 900 K for DLS PCM devices assuming interface heating. For bulk heating, the power required decreases with length, since less volume is heated. For interface heating, the power required does not change with length because the heat transfer length is much smaller than L_{heater}. Using the DLS shows a 59% and 36% reduction in reset power required compared with devices using SiO_2 as the insulator for bulk and interface heating, respectively.

simulate the effect of contact resistance and 2) the heat generated in the bulk of the phase-change region. In addition, any potential heating from the contact thermoelectric effect could be lumped with the contact resistance heating. Heating may have also occurred in the bulk W, but the measured resistance of W only lines (identical to devices except without the W etch/ GST deposition step) was significantly lower than the PCM devices. Also, SThM measurements did not show a temperature change in the bulk W region, thus the energy consumed by the W was likely not significant.

Fig. 9(b) and (d) shows the simulated temperature change due to bulk heating for SiO_2 and DLS films, respectively. In the case of bulk heating, most of the heat is dissipated through the insulator stack and thus, the thermal resistance is inversely related to the insulator thermal conductivity. Since the thermal resistance represents the temperature change generated per applied power, this means that the insulator thermal conductivity linearly decreases the energy required to switch. The simulations are in agreement with the analytical estimation, showing a 59% reduction in power to reach the melting temperature for DLS devices compared with the SiO_2 devices. This is in good agreement with the measured energy reduction attained between the SiO_2 and DLS devices. Another important detail to note is the decrease in total power required to reach the melting temperature with L_{heater} length. Fig. 10(a) shows the relative power required to reach the melting temperature in the bulk for various dimensions. Since the volume heated decreases linearly with L_{heater} length, the required power linearly decreases as well. For interface heating, Fig. 9(c) and (e) show the simulated temperature change due to interface heating for SiO_2 and DLS films, respectively. For this case, the heat travels along the GST and W layers while gradually dissipating into the insulator, similar to a thermal fin. A thermal healing length $L_{thermal}$ can be calculated which is the transfer length of the temperature profile and describes the relationship between the thermal conductivity of the insulator, $k_{insulator}$, and the metal, k_W, as follows:

$$L_{thermal} \propto \sqrt{\frac{k_W}{k_{insulator}}}. \quad (5)$$

Thus, the effective volume heated is larger if the insulator thermal conductivity decreases. As a result, the simulated reduction in power is 36% for DLS devices compared with SiO_2 devices. The temperature profile near the GST/W interface was identical for $L_{heater} = 2, 5$, and 10 μm devices, since the thermal length was ∼100 nm, thus $L_{thermal} \ll L_{heater}$. In addition, since the volume heated remains constant with device length, the relative power did not depend on L_{heater} as shown in Fig. 10(b). Simulating only interface heating does not agree with the measured results for both reduction in power from changing the insulator and changing L_{heater}. Thus, the required energy to switch is consumed mostly with heating up the bulk, rather than heating the switching region at the interface.

The relative energy generated in the two locations can be approximated by assuming that the current is the same for both the bulk GST and the interface region. Thus

$$E_{interface}/E_{bulk} = R_{interface}(T_{interface})/R_{bulk}(T_{bulk}) \quad (6)$$

where E_x is the energy at location x and $R_x(T_x)$ is the electrical resistance at temperature T and location x. For the bulk GST region, the resistance decreases over five orders of magnitude as the temperature increases [1]. Thus, the bulk GST region likely consumes a large part of the energy, despite not being the switching region. The interface resistance, however, is less dependent on temperature [27]. Thus, as the bulk heats up and becomes more conductive, gradually more energy is generated at the interface. Therefore, the highest temperature and switching occur at the interface.

The energy required to switch the PCM device can be used as an upper bound for the volume switched. If there is no energy lost to the surroundings, the energy to heat the phase-change layer to the melting temperature and the latent heat of

melting is ∼1.2 aJ/nm^3 [28]. For 18 pJ, the energy required to switch the DLS $L_{\text{heater}} = 2$ μm device, the volume melted must be below 1.5×10^7 nm^3 or melted length < 1.5 μm for the devices used in this paper. Thus, it is impossible for the entire bulk GST region to be melted and the GST must be switching at the interface. The devices in this paper show much lower energy and reset current density than other reported devices of similar dimensions (typically ∼10 nJ and ∼10 MA/cm^2) [4], [17]. Further thermal confinement in the insulators can reduce the reset energy and will continue to show significant benefit for all device structures, including confined cells where the primary heat loss path is into the insulator [16].

V. Conclusion

This paper utilized the planar confined PCM device to reduce the volume melted, and a thermally resistive multilayer insulator SiO_2/Al_2O_3 to achieve low reset energy in PCM devices. Reset energies as low as 18.25 ± 15.8 pJ and current densities of 0.94 ± 0.51 MA/cm^2 were measured for a contact area of A = 10^4 nm^2 and heater/GST length of $L_{\text{heater}} = 2$ μm. SThM and Raman mapping suggest that the phase-change region near the heater/GST interface exhibits the highest temperature change and thus represents the switching region. Simulations and analytical models show that most of the energy is used to heat the bulk GST region until the heater/GST contact resistance begins to dominate, at which point the heating and thus switching occurs near the interface. The thermally resistive DLS devices show a strong 60% reset energy reduction and a path to further reduce reset energy via thermal confinement in the insulator.

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