Probing Self-Heating in RRAM Devices by Sub-100 nm Spatially Resolved Thermometry

Sanchit Deshmukh, Miguel Muñoz Rojo, Eilam Yalon, Sam Vaziri, Eric Pop
Electrical Engineering, Stanford University, Stanford, CA 94305, U.S.A. | Contact: epop@stanford.edu

Resistive memory (RRAM) is a promising technology for high density, non-volatile data storage. Metal-oxide RRAM involves forming and breaking conductive filaments (CF) in an oxide like HfO_2 as the mechanism of data storage. CFs are sub-50 nm in diameter [1], causing sharp temperature gradients within the RRAM oxide. However, imaging individual CFs in RRAM devices is challenging due to their nanoscale size and the presence of the top electrode (TE). While previous works have performed electrical [2] or optical averaging [3] of CF temperature, evaluating the heating of a single CF within RRAM has remained an open problem.

Here, we measure the temperature rise (ΔT) at the top surface of TiN/HfO_2/Pt and Pt/Ti/TiN/HfO_2/Pt RRAM devices (**Fig. 1a**) by scanning thermal microscopy (SThM) [4] (**Fig. 1b**). We also used Raman thermometry [5,6] (**Fig. 1c**) to measure surface temperature of a device, subsequently comparing with the extracted SThM temperature readings. Devices have different TE thickness (20 nm TiN, 2 nm Ti/33 nm Pt and 20 nm TiN/35 nm Pt) to understand its effect on the measurement resolution and device behavior.

We form all devices at ~1 μA compliance and they switch multiple times electrically (**Fig. 2**). **Fig. 3a** shows the SThM thermal map on the TE surface of a 55 nm TE device. In the low resistance state (LRS) of our devices, the SThM clearly images a hot spot, which is the thermal signature of the underlying non-volatile CF. We note this heating is probed ~60 nm (thickness of TE plus thin Al_2O_3 capping) above the CF, revealing a hot spot < 200 nm due to heat spreading in the TE. After the devices are reset to their high resistance state (HRS), no hot spot is detected. We vary the power applied to the device by changing the steady state DC bias from 0 to ~ ±1 V. We repeat the measurement on devices with different TE thickness, formed under similar conditions. The SThM images show increased heating with increasing power (at LRS) while the hot spot width remains unchanged for the same TE thickness. The width of the hot spot decreases with decreasing TE thickness (**Fig. 3b**), indicating effect of heat spreading in the TE, and actual heat generation in a sub-100 nm CF diameter.

The SThM uses a thermo-resistive element, relating changes in the electrical resistance of the probe (mV) with temperature, requiring calibration of the mV signal. To calibrate our SThM heat maps, we measure the same devices with Raman thermometry, enabled by a monolayer of MoS_2 transferred on top of the TE and acting as an ultra-thin thermometer [6] (**Fig. 1c** and **Fig. 3c**). We note that the spatial resolution of the Raman measurement is limited by the laser spot size (~0.4 μm) resulting in an averaged signal (**Fig. 3c**).

We perform calibration (below the Raman spatial resolution limit) for sub-100 nm features using a set of metal line heaters/thermometers with widths varying between 50 nm and 750 nm, where the metal temperature rise (ΔT) can be accurately measured by electrical thermometry. We measure a line-width-dependent conversion factor (**Fig. 4a**), ultimately letting us estimate CF heating with sub-100 nm resolution. The calibration approach does not decouple interference from the topography signal of the heater lines at sub-50 nm dimensions, which presently limits the extracted temperature accuracy and spatial resolution.

The extracted CF hot spot temperature increases with increasing power (P) applied to the RRAM device (**Fig. 4b**). We observe hot spot peak $\Delta T \approx 50$ K (**Fig. 4c**) for $P = 0.75$ mW at the TE top surface, which is higher than that measured by Raman thermometry shown in **Fig. 3c** at similar power. This is due to spatial averaging of the Raman signal vs. the sub-100 nm resolution of the SThM. While this temperature is measured at the TE surface, the CF temperature is far higher, as seen from simulations (**Figs. 5a & 5b**), and depends strongly on the filament diameter d_{fil} (**Fig. 5b**). The hot spot temperature is higher as we lower the TE thickness for the same power (**Fig. 6**), as a thinner TE enables probing closer to the filament. The filament ΔT is high for the same values of power, and an even thinner TE with less series resistance than TiN could aid in probing a few nm away from the filament using this approach.

In summary, we used SThM to probe RRAM device temperatures with sub-100 nm spatial resolution for the first time. Such direct measurements of filamentary self-heating in RRAM devices open the doors for thermal engineering of energy-efficient non-volatile memory. This work was supported by Stanford NMTRI.

Ref: [1] U. Celano et al. *Nano Lett* **15**, 7970 (2015). [2] E. Yalon et al. *TED* **62**, 2972 (2015). [3] S. Kumar et al. *Nat. Comm* **8**, 658 (2017). [4] A. Majumdar et al. *Ann Rev Mat Sci* **29**, 505 (1999). [5] E. Yalon et al. *Sci Rep* **7**, 15360 (2017). [6] E. Yalon et al. *Nano Lett* **17**, 3429 (2017).

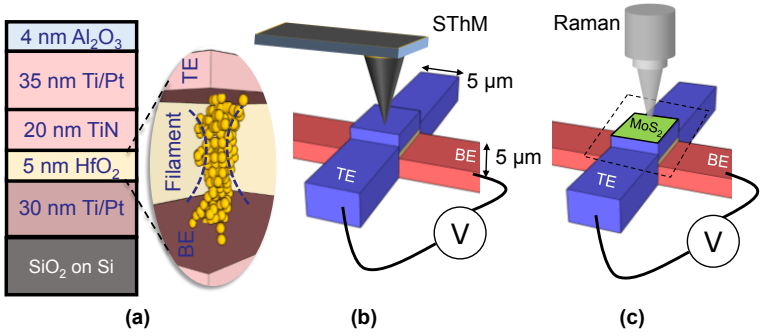

Fig. 1. (a) RRAM device schematic showing 5 nm HfO_2 as switching layer with the inset showing a single filament. Devices are capped with Al_2O_3 for electrical isolation. **(b)** Schematic for Scanning Thermal Microscopy (SThM) tip scanning over device with bias. **(c)** Raman laser scanning over device with transferred MoS_2 capping layer for thermal sensing.

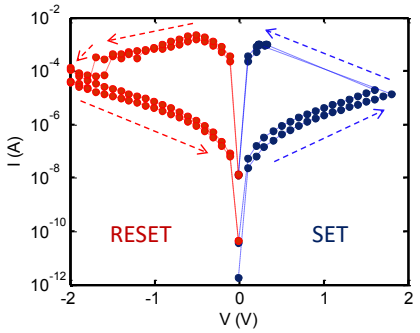

Fig. 2. Typical switching *I-V* characteristics for the 55 nm TE devices. 55 nm TE devices switch multiple times. 20 nm TE devices cannot reset due to the high series resistance of TE.

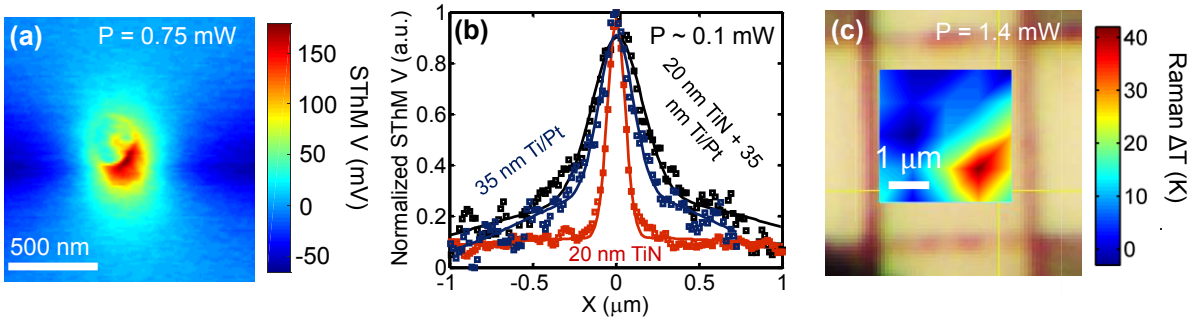

Fig. 3. (a) SThM image of a single filament imaged through the top of the 55 nm thick TE (and 4 nm Al_2O_3 capping). **(b)** Normalized SThM V at TE surface for different TE at $P \sim 0.1$ mW; **(c)** Raman thermometry of device in Fig. 3a, using MoS_2 monolayer as Raman active layer, acting as an ultrathin thermometer (also see Fig. 1c).

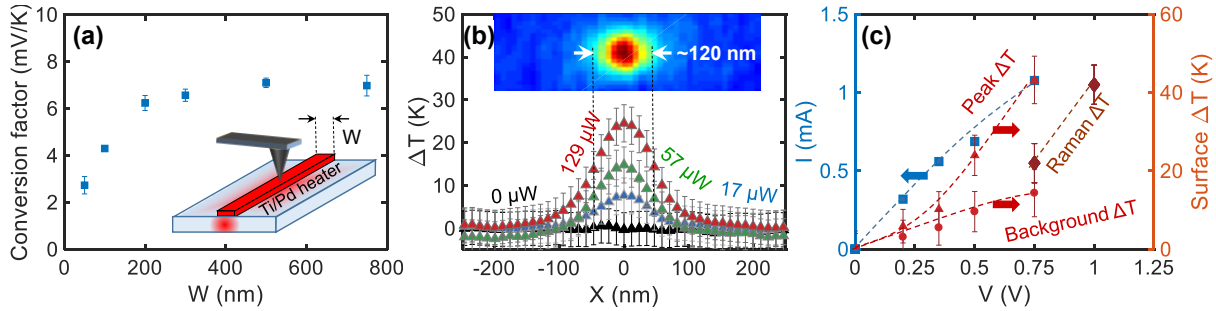

Fig. 4. (a) Conversion factor for SThM in mV to heater temperature in K, measured on Ti/Pd heaters of widths 50 nm to 750 nm. **(b)** Extracted SThM ΔT at TE surface with increasing power for 20 nm TiN TE, inset shows ΔT map. **(c)** Extracted SThM surface peak ΔT at center of hot spot and background ΔT, Raman peak ΔT and I vs V for 55 nm TE.

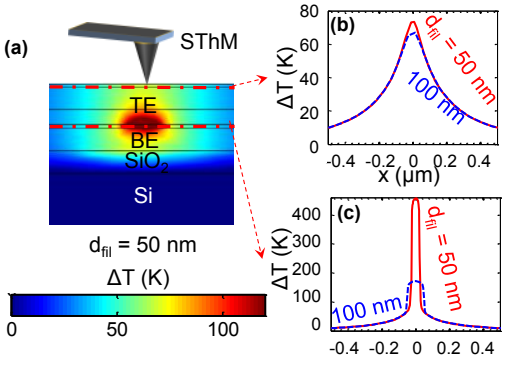

Fig. 5. (a) COMSOL simulation of RRAM device stack at $P = 1$ mW. SThM measurement is on top of the TE (& Al_2O_3). **(b)** Expected TE top surface ΔT for $d_{fil} = 50$, 100 nm. **(c)** Much larger expected filament ΔT for $d_{fil} = 50$, 100 nm.

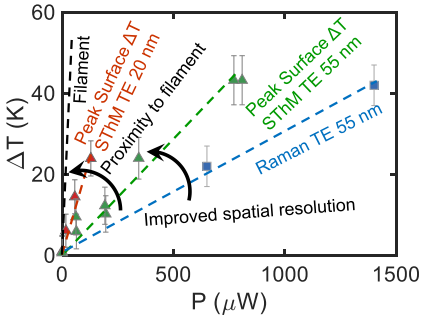

Fig. 6. Extracted SThM peak surface ΔT at the center of the hot spot & Raman thermometry peak surface ΔT. Actual filament ΔT is higher.

978-1-5386-3028-0/18/$31.00 ©2018 IEEE