Localized Heating in $MoTe_2$-Based Resistive Memory Devices

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Layered materials like transition metal dichalcogenides (TMDs) and hexagonal boron nitride (h-BN) have been recently demonstrated as the switching layers in resistive random access memory (RRAM) devices [1-3], but their switching mechanisms are not yet well understood. In this work, we show resistive memory switching in $MoTe_2$ devices and investigate the thermal origins of their switching behavior using scanning thermal microscopy (SThM). We observe localized heating due to the formation of a conductive plug, which is correlated with electro-thermal simulations, providing the first thermal insights into the operation of such RRAM devices.

We fabricated vertical $MoTe_2$ devices (**Fig. 1a-b**) using mechanically exfoliated $MoTe_2$ crystals grown by chemical vapor transport (CVT). Thin $MoTe_2$ was transferred onto Ti/Au (5/40 nm) bottom electrodes (BE) patterned by electron beam (e-beam) lithography and deposited by e-beam evaporation. We patterned and e-beam evaporated SiO_2 (65 nm thick) onto part of the $MoTe_2$ to isolate the Au bottom and top electrodes (TE). The Au TEs (80 nm thick) were then patterned and evaporated onto the $MoTe_2$, and the devices were capped with ~10 nm Al_2O_3 by atomic layer deposition (ALD) [4]. We performed all exfoliation, transfer, metal lift-off, and ALD steps in a N_2 glove box with <3 ppm O_2 and H_2O, to prevent degradation of the $MoTe_2$.

Fig. 1c displays current-voltage (*I-V*) measurements of forming in two devices (Devices 1 and 2). A series resistor was used to limit the current through the device during forming. After the initial forming step the devices show bipolar switching between low and high resistive states (LRS and HRS), as shown in **Fig. 1d**, which is representative of ~20 vertical $MoTe_2$ devices we measured.

Scanning thermal microscopy (SThM) measurements were performed on the surface of Device 1 in the LRS after the forming step. SThM is an atomic force microscope (AFM) based technique that uses a thermally resistive probe to obtain heating maps of a device under bias with nanoscale resolution [5]. **Fig. 2a** shows optical and AFM topographic images of the TE region (capped with Al_2O_3). **Fig. 2b** shows a schematic of the SThM setup on the device geometry. **Figs. 2c-e** display SThM images taken at 0.25 V, 0.5 V, and 0.65 V between the TE (applied voltage) and BE (ground). The colorbar shows the output SThM voltage, which is proportional to the temperature rise ΔT. At low voltage (0.25 V), a hot spot appears (see **Fig. 2c**). At higher voltages (0.5 V and 0.65 V) the hot spot grows larger and is clearly observed on the Au TE, revealing localized heating in the device (see **Figs. 2d-e**). This localized heating suggests the formation of a conductive plug. Importantly, these SThM measurements provide direct evidence that the switching mechanism is a thermally-activated process such as localized phase change [2], defect (i.e. vacancy) generation, or Te migration in the $MoTe_2$ [6].

Next, we used three-dimensional (3D) simulations to estimate the device ΔT during operation, as the (surface) SThM does not give a direct measurement of the (buried) plug. We considered lower and upper bounds of 100 and 1000 (based on the resistance change in the devices) for the ratio (r_σ) between the electrical conductivity in the $MoTe_2$ plug and the film. **Fig. 3a** shows a temperature profile of a cross-section of the device for a conductive plug diameter of 300 nm and r_σ = 100. As expected, the hottest part of the device is the conductive plug, while the top and bottom surfaces are much cooler due to heat dissipation in the electrodes and in the substrate. **Fig. 3b** shows the simulated ΔT of the device vs. power for two plug diameters (0.25 and 1 μm) and r_σ = 100. **Fig. 3c** shows simulated ΔT of the conductive plug and the top surface of the device vs. plug diameter at different power inputs and r_σ. From a preliminary analysis, we estimate that the peak ΔT of the top surface of the device with a power input of 2.5 mW, i.e. similar to our experimental conditions, ranges from ~23 to 60 K, depending on the conductive plug diameter and r_σ. We note that the corresponding plug temperature is more sensitive to diameter than the surface temperature, resulting in a larger plug temperature range (see **Fig. 3c**).

In summary, we observed localized heating in $MoTe_2$-based memory devices for the first time, pointing to the temperature-activated switching mechanism. This work was supported in part by the NSF-EFRI 2-DARE program, the Stanford NMTRI, and a NDSEG fellowship (I.M.D.). We acknowledge assistance with $MoTe_2$ growth from Ian Fisher and Hsueh-Hui Kuo.

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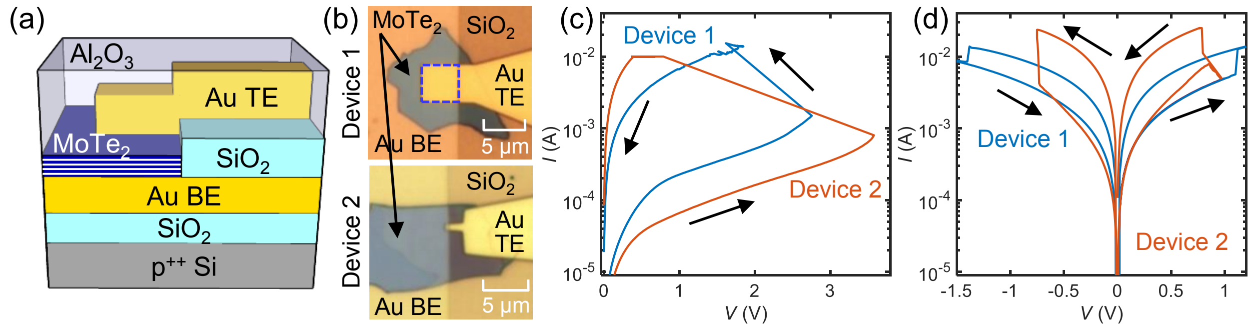

Fig. 1: (a) Schematic of vertical $MoTe_2$ memory devices with Au top and bottom electrodes (TE and BE, respectively) and SiO_2 isolation layers. (b) Top view optical images of two devices, Device 1 (~30 nm thick $MoTe_2$) and Device 2 (~55 nm $MoTe_2$), with top electrode areas of 4.5 × 4.5 µm² (dashed outline) and 0.7 × 0.4 µm², respectively. (c) Measured *I*-*V* curves showing forming of Devices 1 and 2, with arrows corresponding to the direction of the voltage sweeps. For all measurements, the voltage is applied to the TE, and the BE is grounded. (d) Measured *I*-*V* curves showing bipolar switching of Devices 1 and 2.

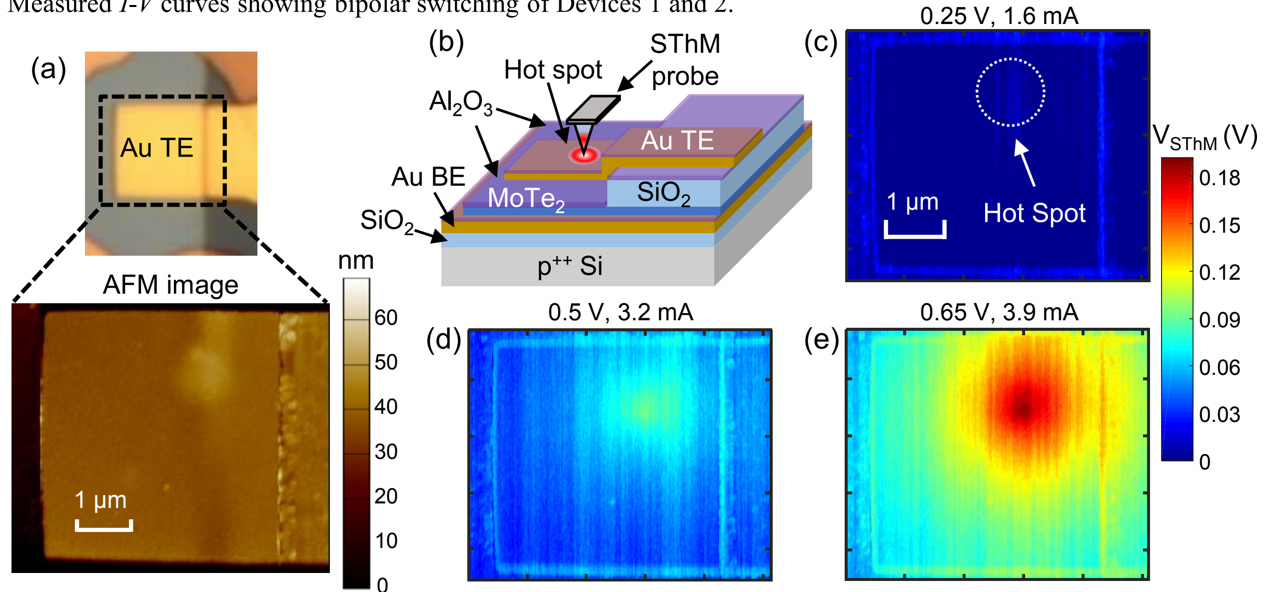

Fig. 2: (a) Optical and AFM images of Device 1 showing the TE region. (b) Schematic of SThM setup showing the probe on the sample surface. SThM images of Device 1 (after forming, in the LRS) at (c) 0.25 V, (d) 0.5 V, and (e) 0.65 V. The colorbar corresponds to the output SThM voltage, which is proportional to temperature rise ΔT. A hot spot (corresponding to the bump on the TE seen in the AFM) is observed as the applied voltage increases, showing evidence of localized heating due to a conductive plug in the device.

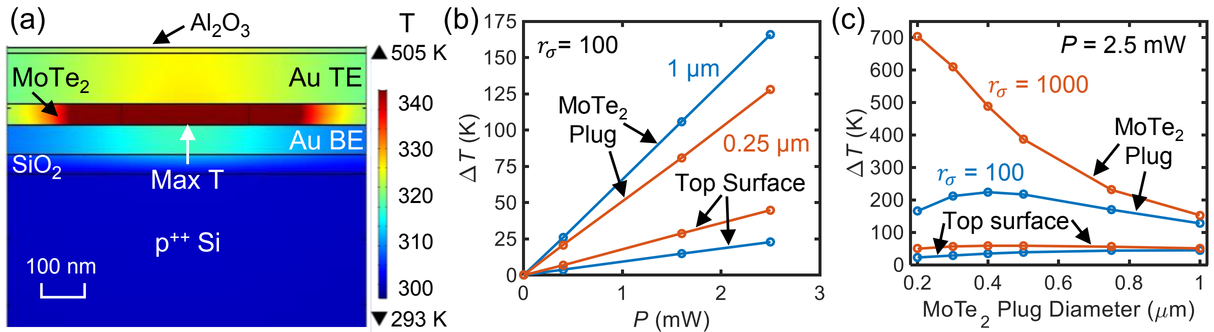

Fig. 3: (a) COMSOL simulation showing temperature profile of device cross-section. The ratio (r_σ) between the electrical conductivity in the $MoTe_2$ film and plug is 100. The simulation was performed at P = 2.5 mW for a $MoTe_2$ plug diameter of 300 nm, showing a maximum temperature of ~500 K. (b) Simulated top surface ΔT vs. P, for two different $MoTe_2$ plug diameters at r_σ = 100. (c) Simulated ΔT vs. $MoTe_2$ plug diameter for P = 2.5 mW at the top surface and inside the $MoTe_2$ plug for different r_σ.

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